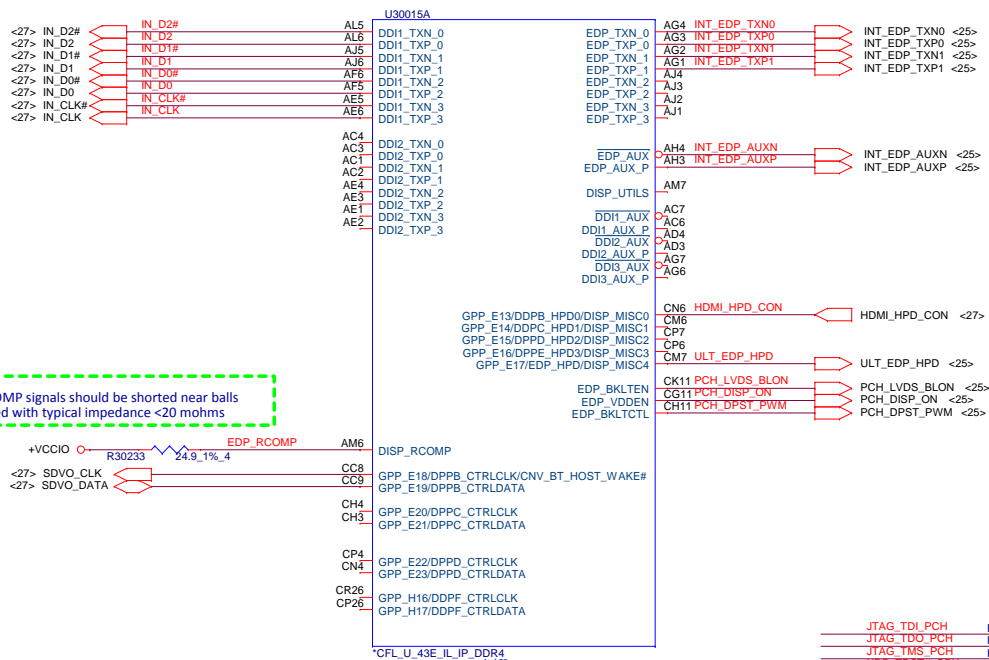


LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : SGND
LAYER 8 : BOT



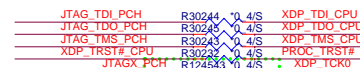
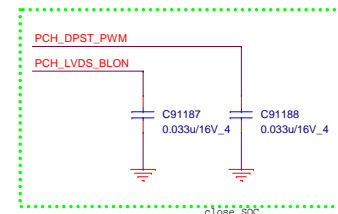
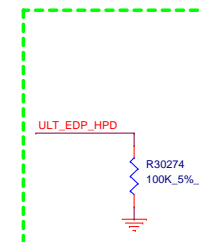
HDMI

+3V <4,10,11,12,13,14,15,17,18,22,25,26,27,28,29,31,32,33,34,35,42,45,46,47>
+1.05V <6,35,41>
+VCCSTPLL <4,5,6,41,42>



DISP_RCOMP signals should be shorted near balls
and routed with typical impedance <20 mohms

Reserve EDP_HPD opposites circuit!

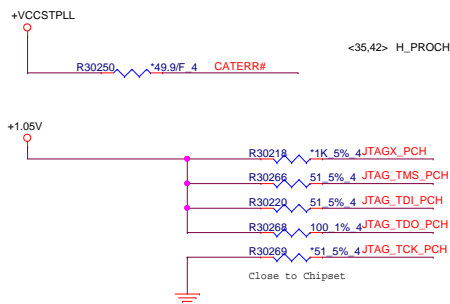


Close to EC



Processor pull-up (CPU)

PLACE NEAR CPU



<35,42> H_PROCHOT#

<35> PM_THRMTRIP#

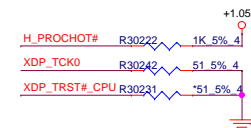
<16> XDP_BPM0

<16> XDP_BPM1

Close to Chipset

4 of 20

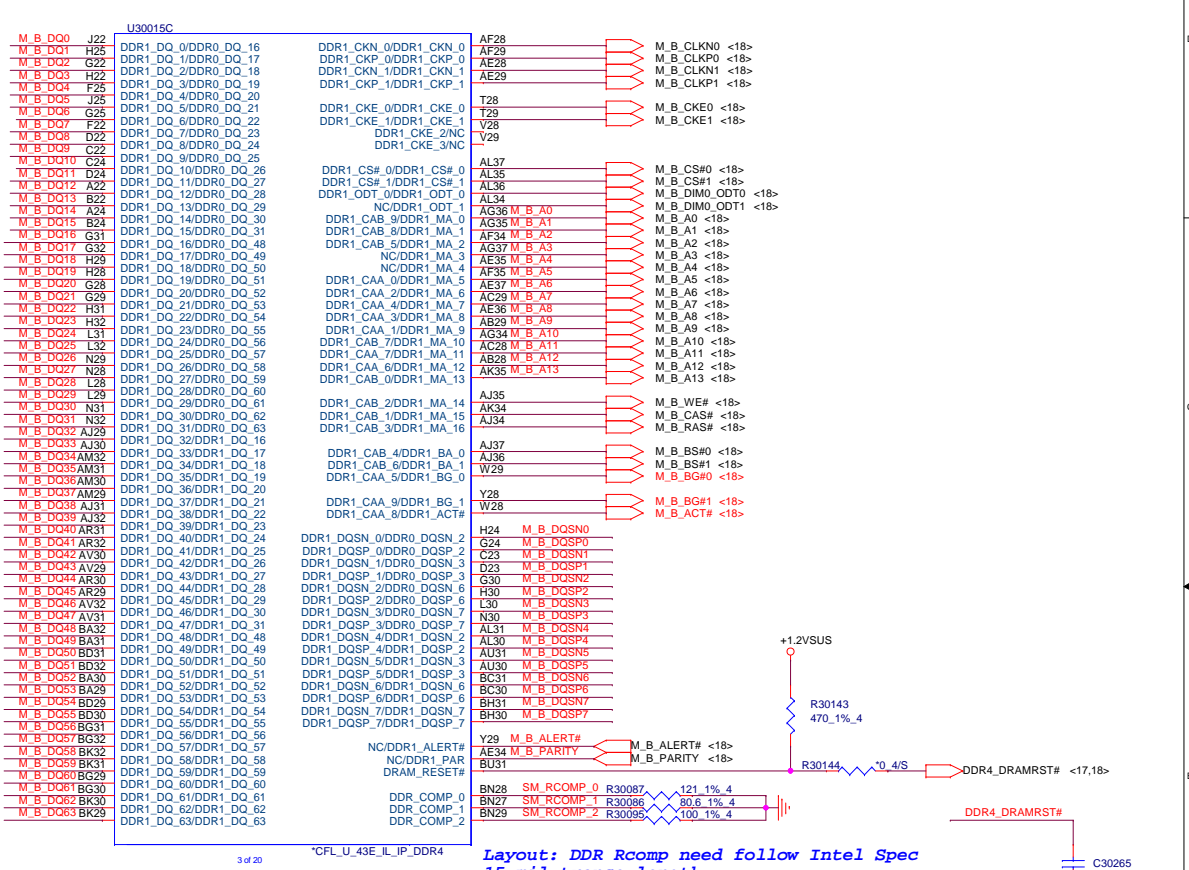
*CFL_U_43E_IL_IP_DDR4

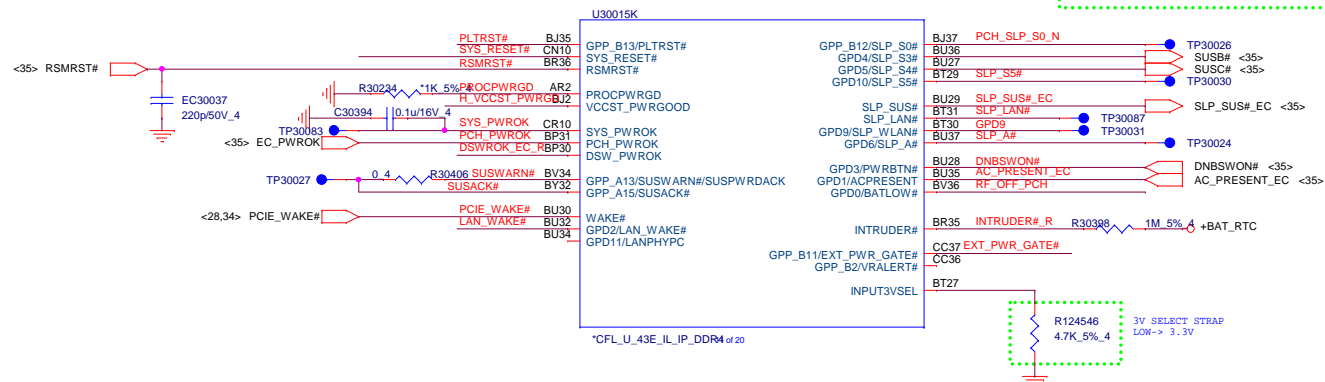
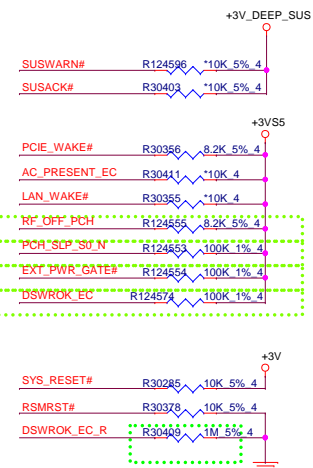
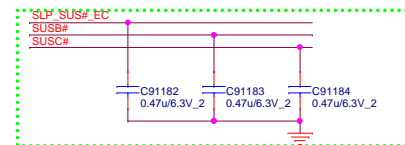
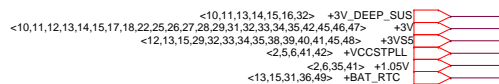


PROJECT : G7BD
Quanta Computer Inc.

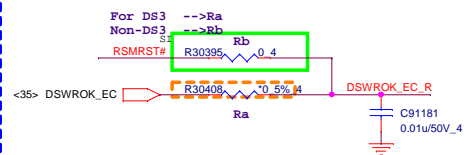
Size	Document Number	Rev
Custom	KBL-U 1/15 eDP/DDI/MISC	1A
Date: Wednesday, December 26, 2018 Sheet 2 of 49		

WHL ULT Processor (MEM-B)





For DS3 Sequence

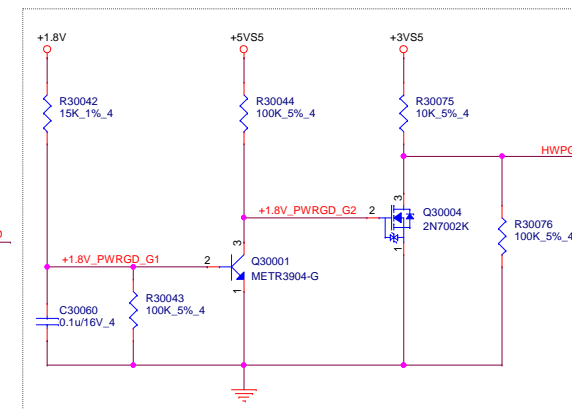
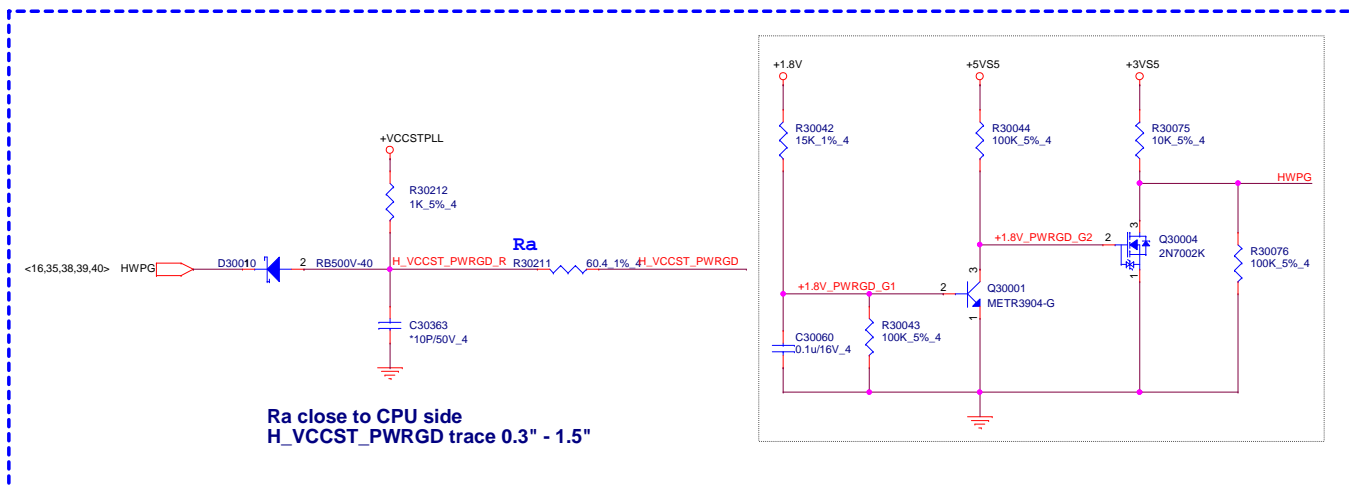
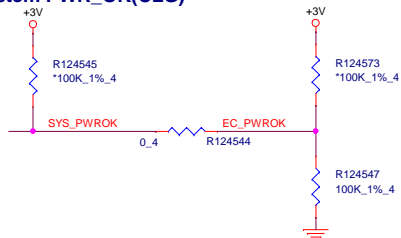


PLTRST#(CLG)

Check Rise/Fall time less than 100ns

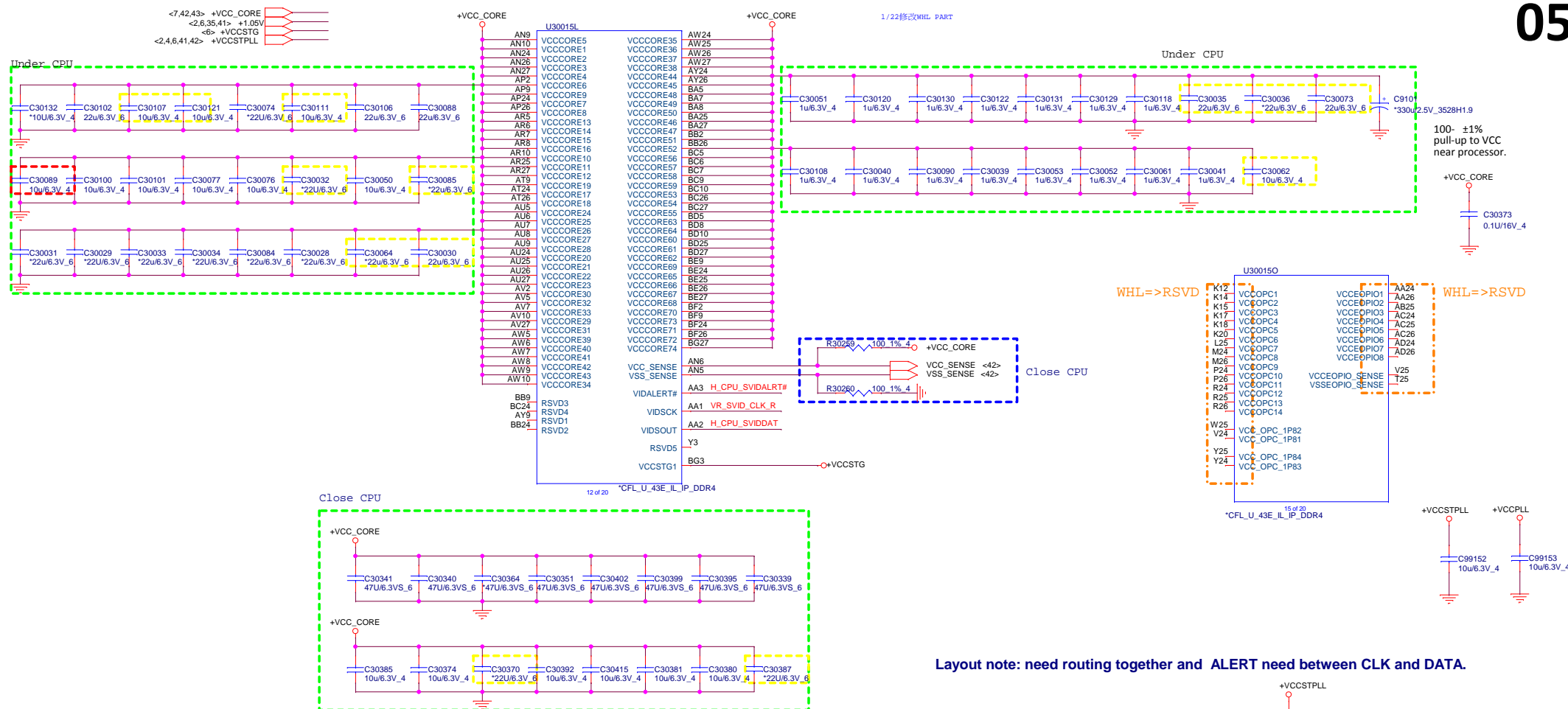


System PWR_OK(CLG)



PROJECT : G7BD
Quanta Computer Inc.

Size Custom	Document Number KBL-U 3/15(PowerManger)	Rev 1A
Date: Wednesday, December 26, 2018 Sheet 4 of 49		



Layout note: need routing together and ALERT need between CLK and DATA.

PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE

CLOSE TO CPU
PLACE THE PU RESISTORS

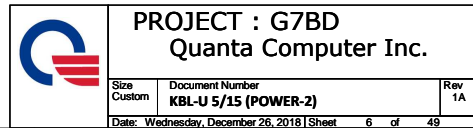
CLOSE TO CPU
PLACE THE PU RESISTORS

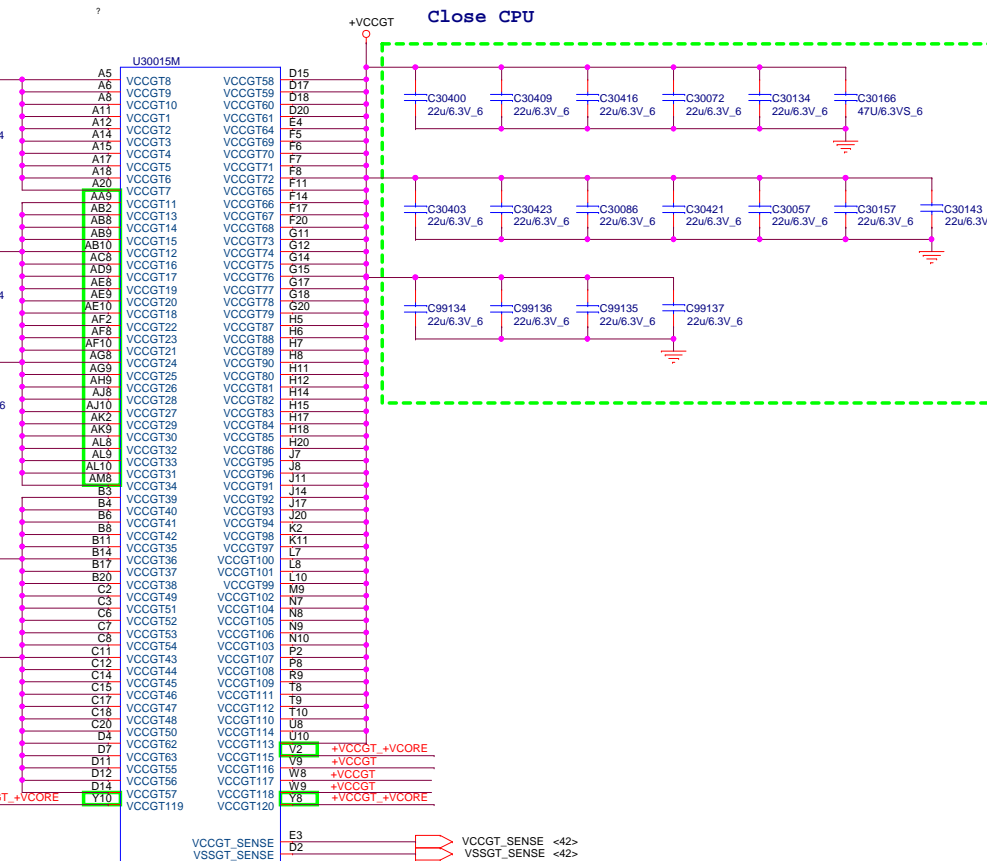
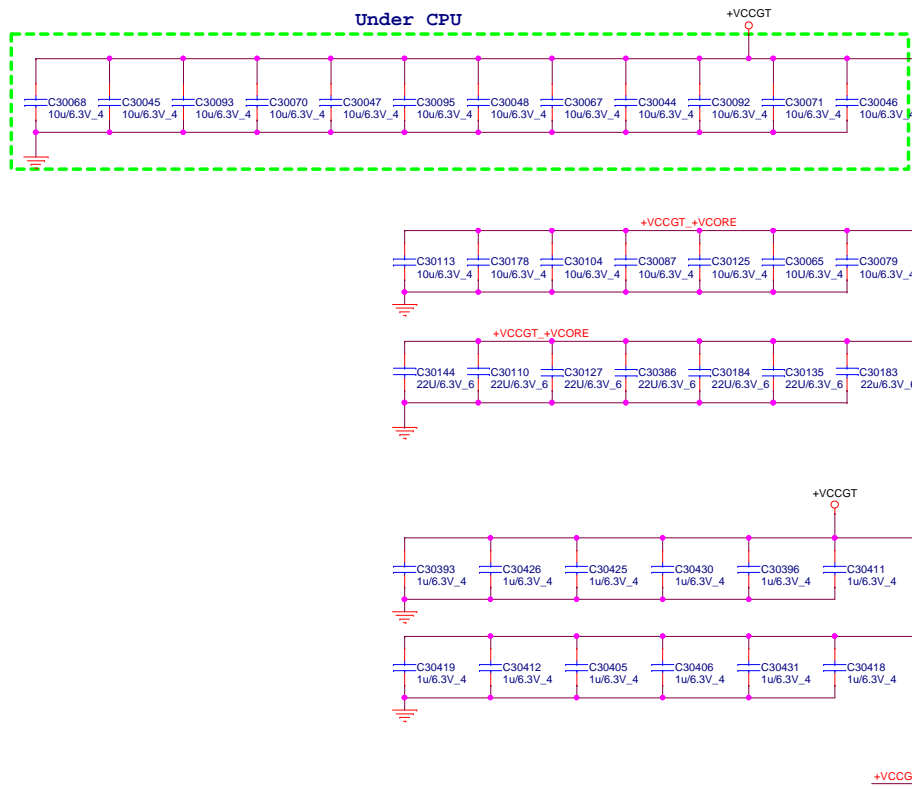
SVID ALERT

SVID CLK

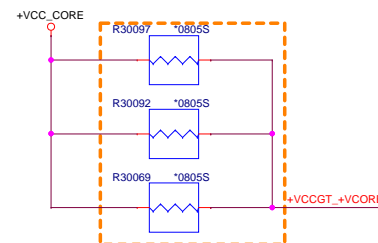
SVID DATA

PROJECT : G7BD Quanta Computer Inc.		
Size Custom	Document Number KBL-U 4/15 (POWER-1)	Rev 1A
Date: Wednesday, December 26, 2018 Sheet 5 of 49		

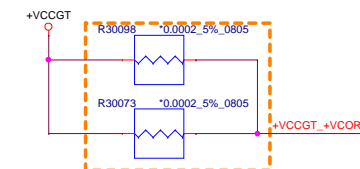




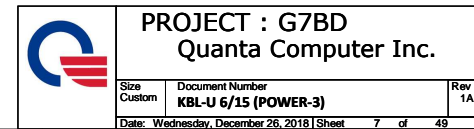
Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

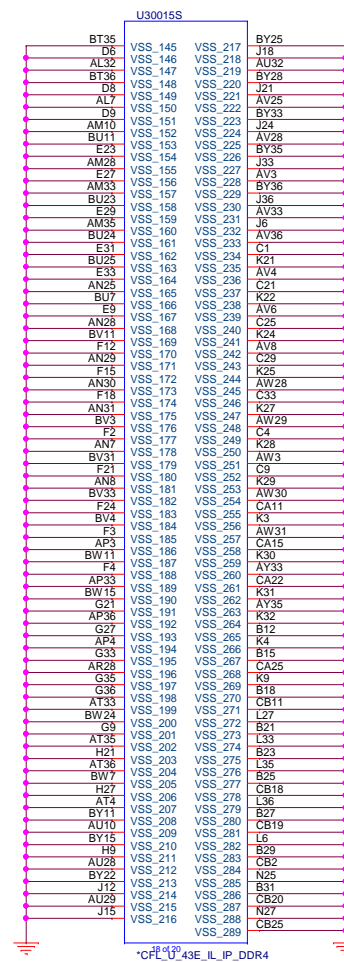
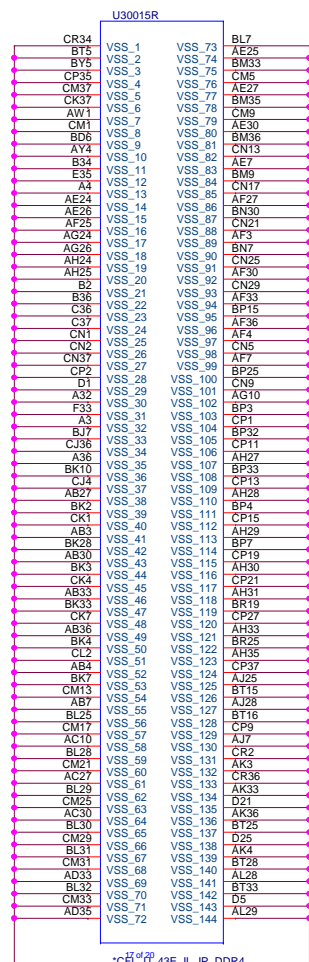
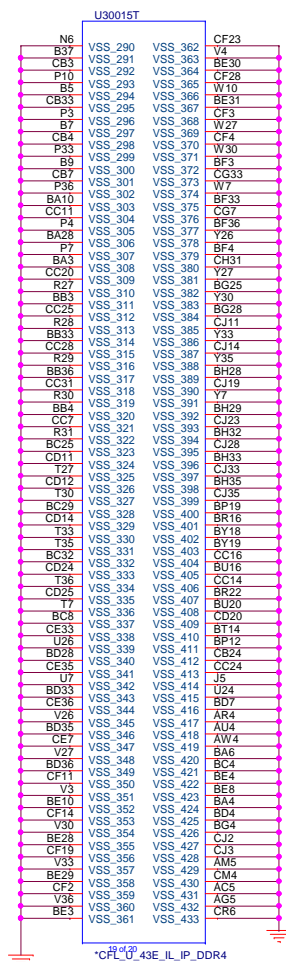


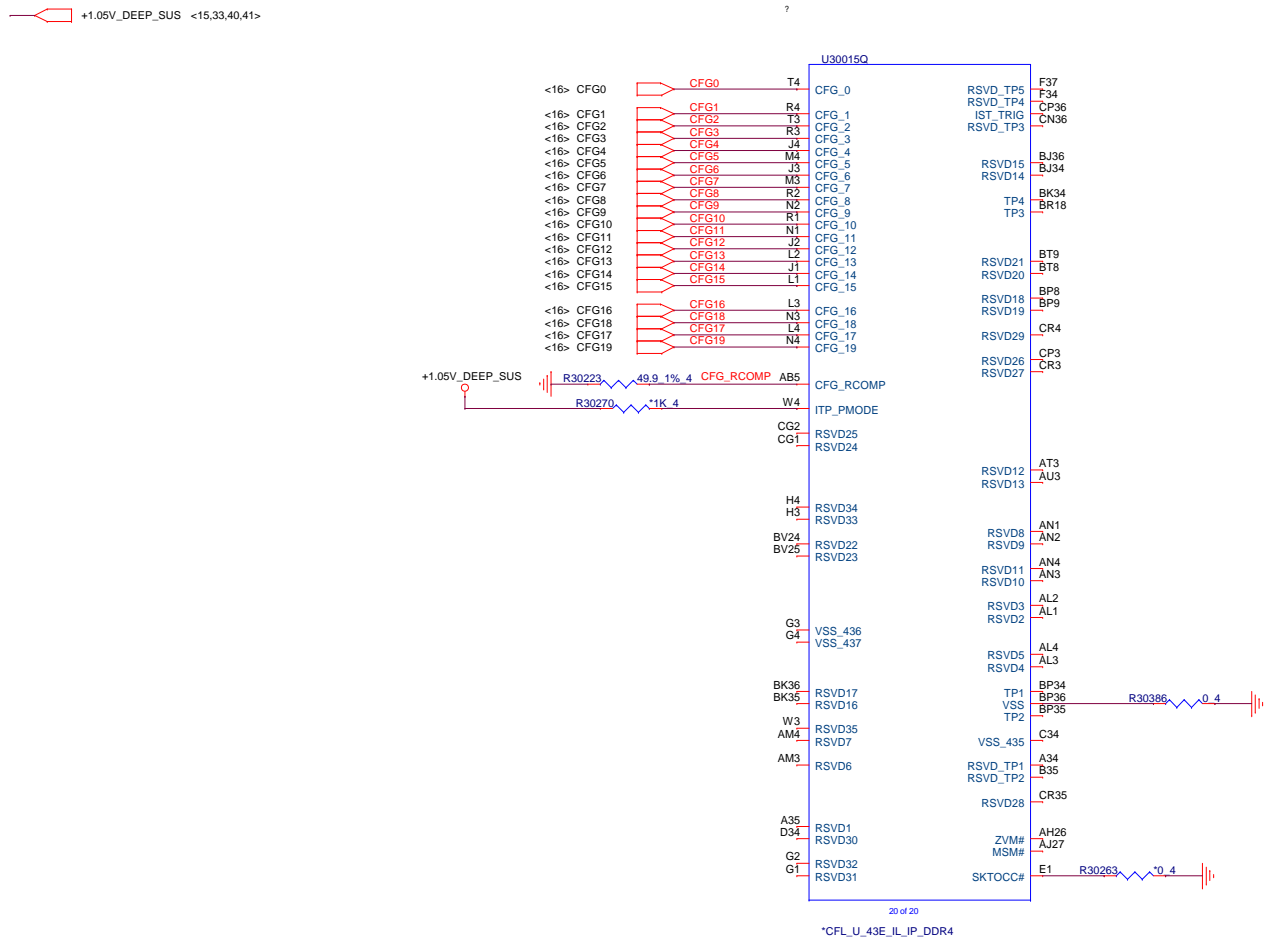
For WHL U42 ES2 上件/0122



For WHL U42 ES1 上件/0122

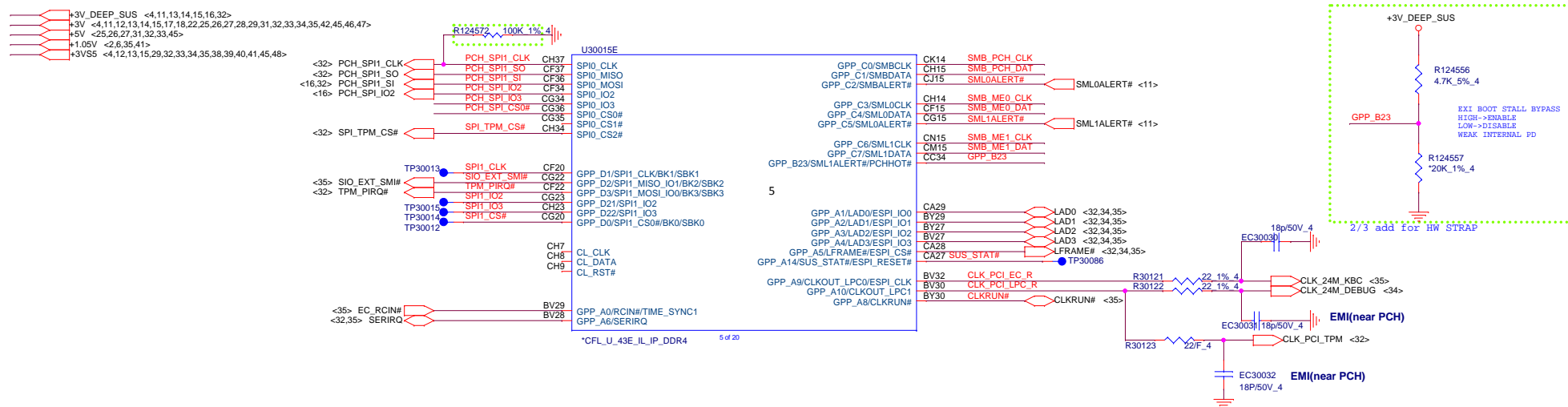




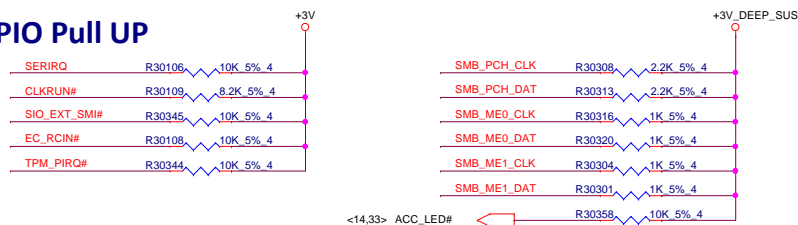


Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	



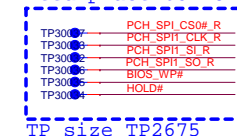
GPIO Pull UP



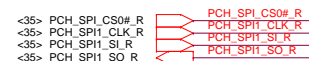
PCH SPI ROM(CLG)

Vender	Size	P/N
MXIC	16MB	AKE3DZN0Z03 (MX25L12873FM2I-10G)
Winbond	16MB	AKE3DF-KN01 (W25Q128JVSQ)
GigaDevice	16MB	AKE3DZN0Q02 (GD25B127DSIGR)
Socket		DG008000011

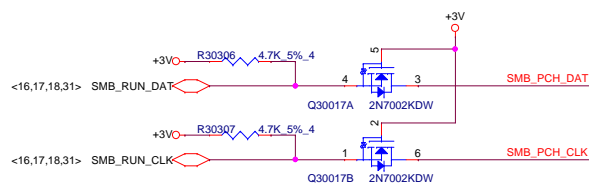
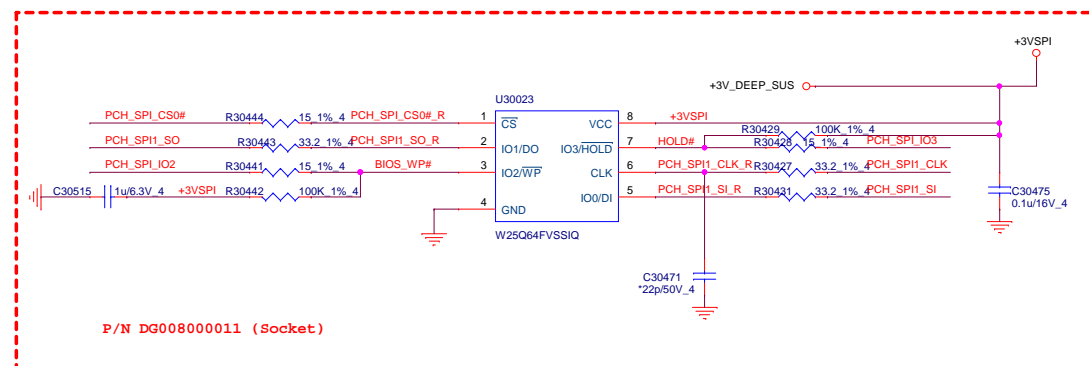
need place to TOP



PCH SPI ROM(CLG)

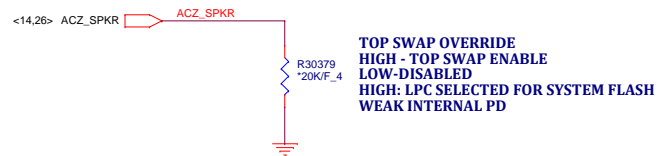


SMBus/Pull-up(CLG)

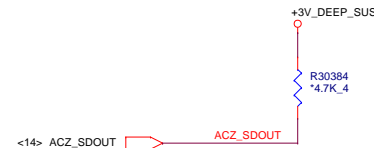
CPU heat pipe local thermal sensor
DDR thermal sensor
ECTouch Pad
XDP
DDR4

Functional Strap Definitions

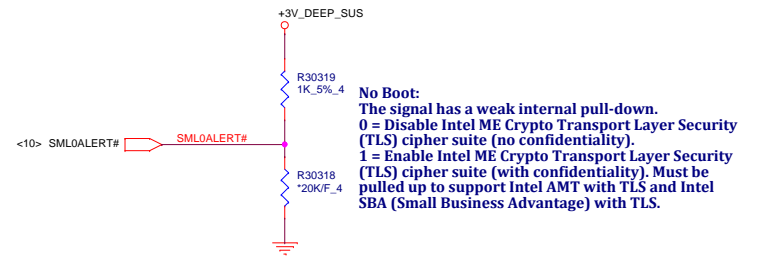
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



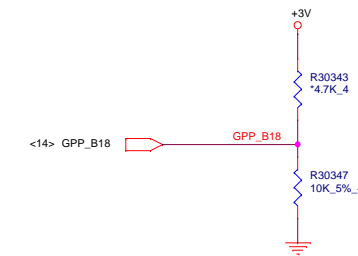
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



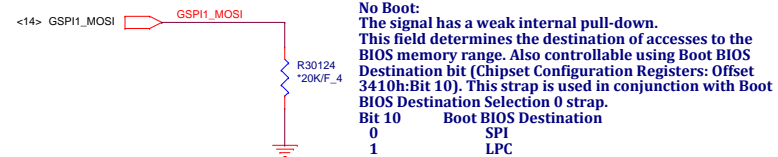
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

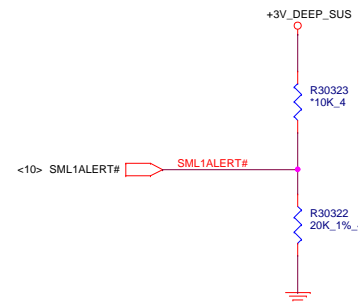


No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

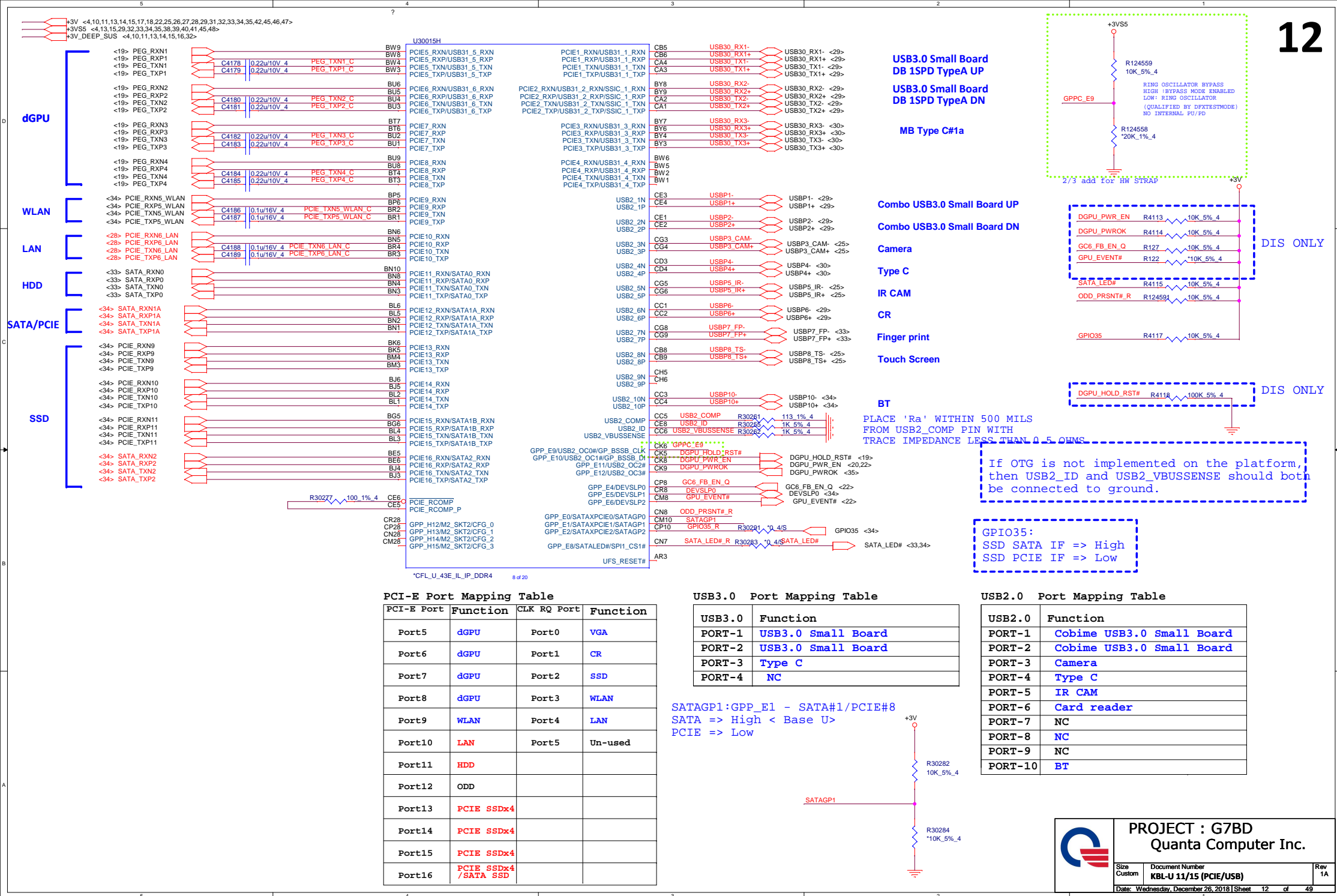


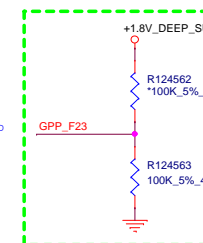
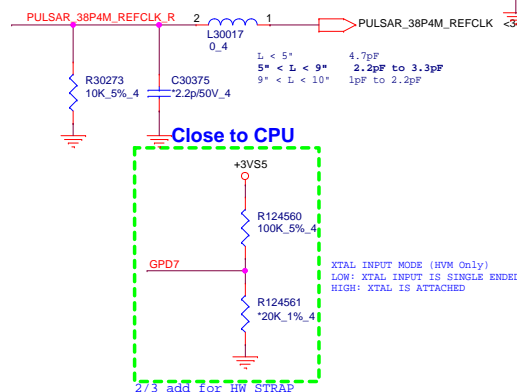
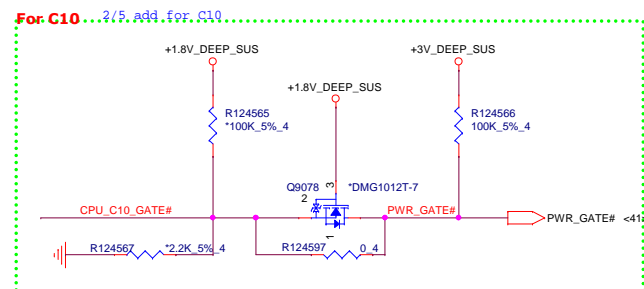
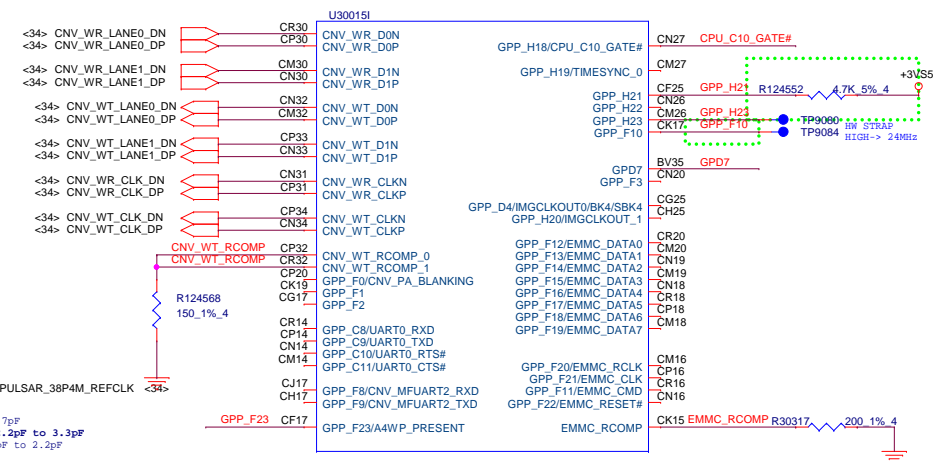
No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.

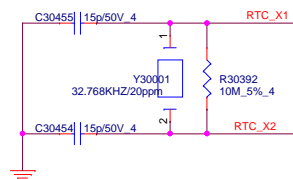




CLK_REQ/Strap Pin(CLG)



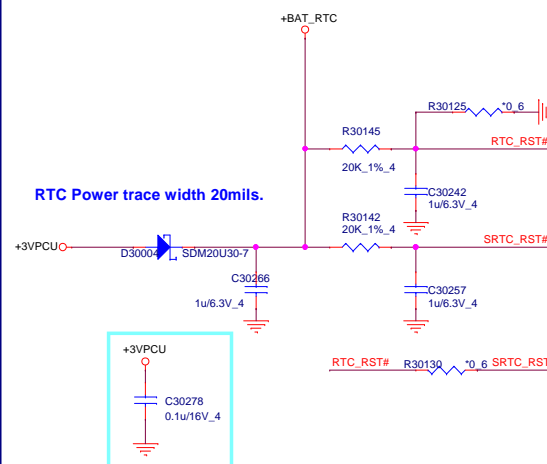
RTC Clock 32.768KHz



RTC Circuitry(RTC)

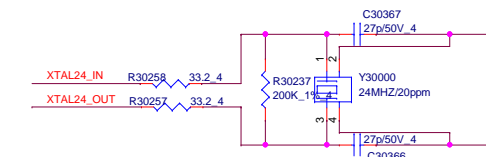
30mils

RTC Power trace width 20mils.



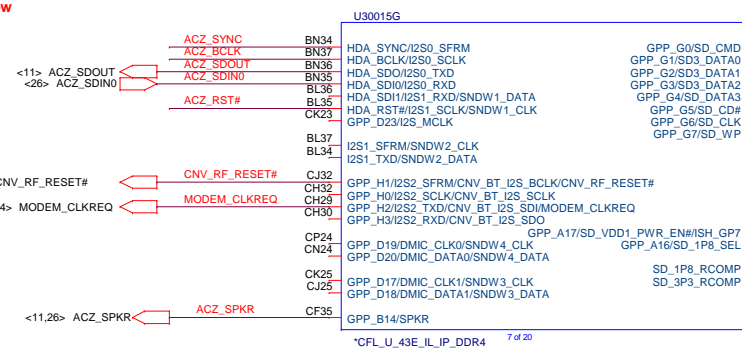
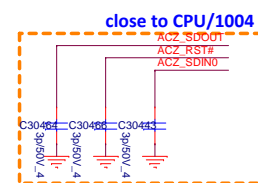
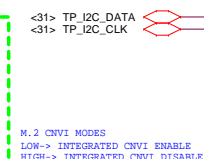
External Crystal

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

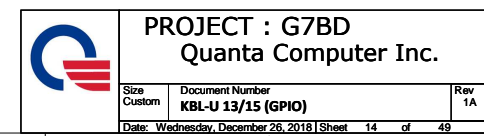


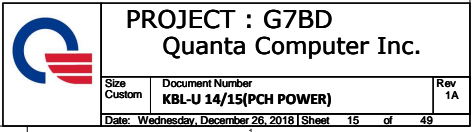
PROJECT : G7BD Quanta Computer Inc.
--

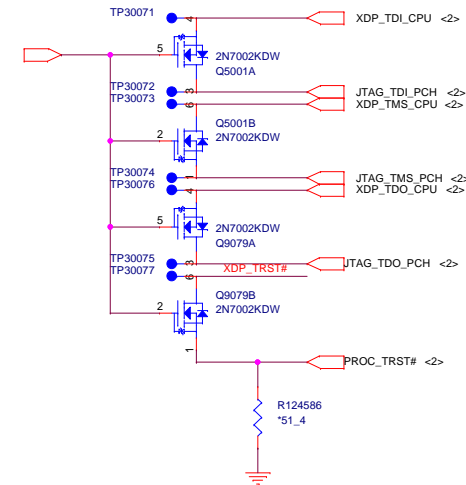
Size Custom	Document Number KBL-U 12/15 (CLK/EMMC)	Rev 1A
Date: Wednesday, December 26, 2018 Sheet 13 of 49		



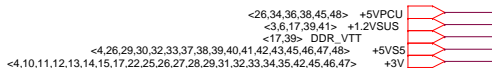
WHL	BOARD_ID[8:7]	Board ID 6	Board ID 5	Board ID 4	BOARD_ID[3:1]		BOARD_ID0
Model	ID8 ID7	ID6	ID5	ID4	ID3 ID2 ID1	ID0	
Definition	Reserve (Default = 00)	0:Finger Print 1:Non-Finger Print	0 : AMD 1 : Nvidia GPU setting	0 : 2G VRAM 1 : 4G VRAM	100 : 14" (WHL) 101 : 15" 1SPD (WHL) 110 : 2SPD (WHL) 111 : 13" (WHL)	000 : 14" 001 : 15 1SPD 010 : MAX-Q 011 : 2SPD	0 : UMA 1 : DIS

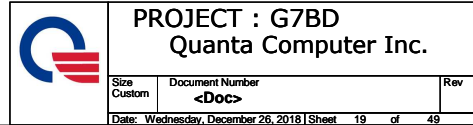


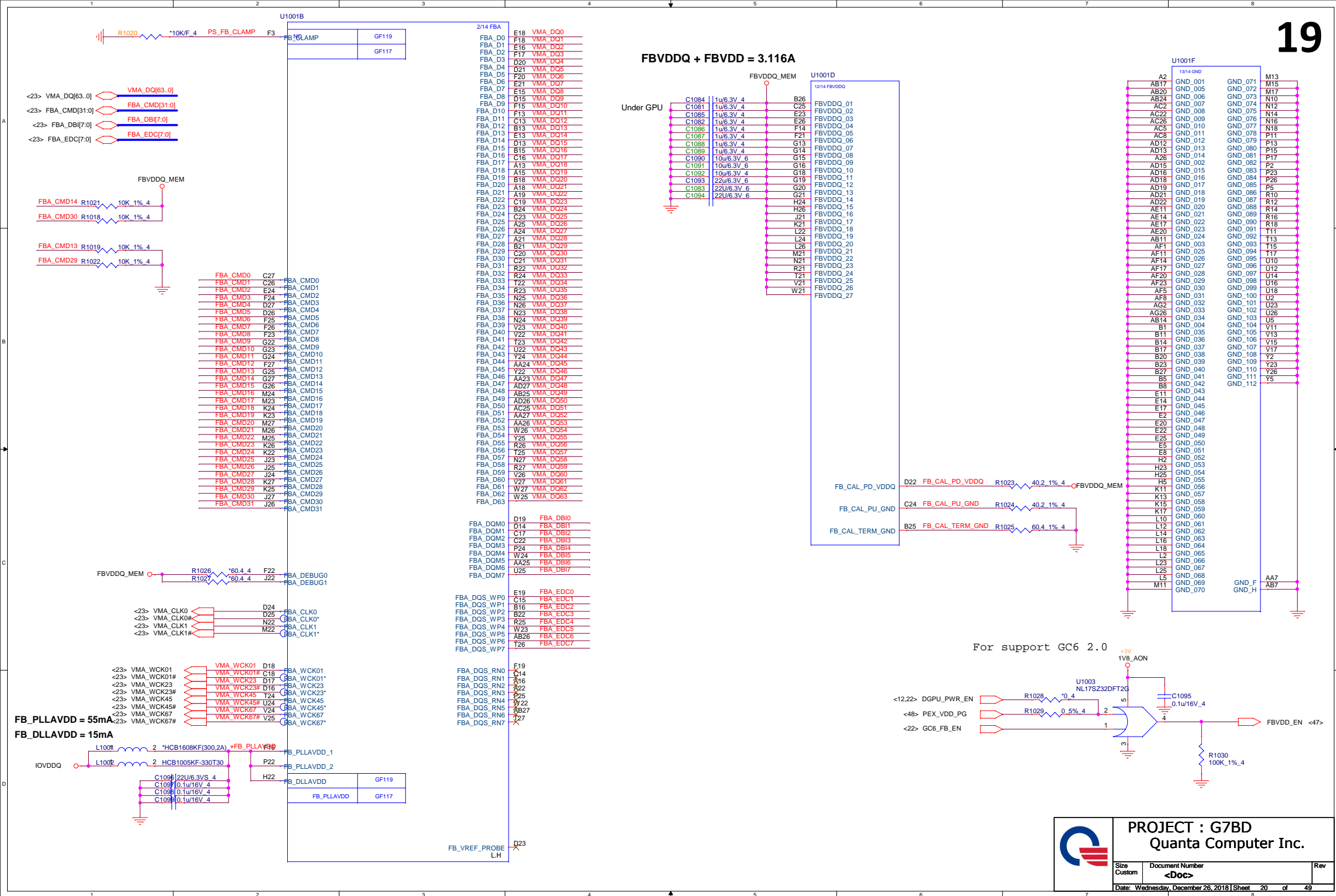












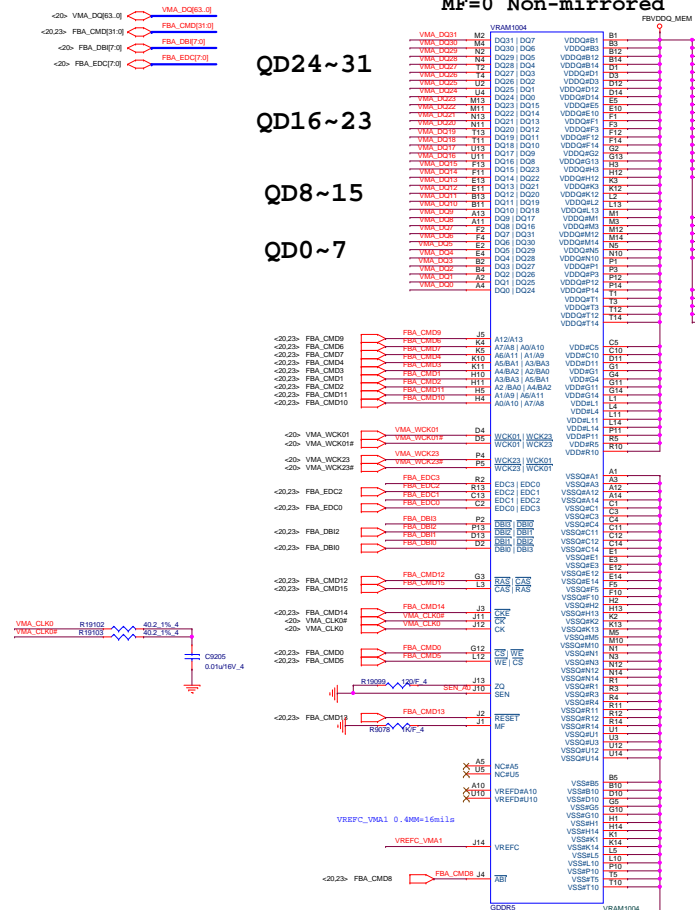
CHANNEL A: 2G GDDR5

Channel A
<0-31>

MF=0 Non-mirrored

Channel A
<32-63>

MF=0 Non-mirrored



<20,21,47> FBVDDQ_MEM 

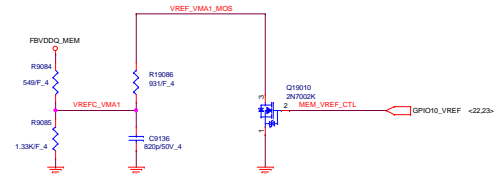
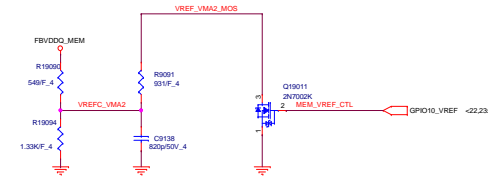
QD56~63

QD48~55

QD40~47

QD32~39

GDDR5 256 x 32	Hynix H5GC8H24MJR-R0C	AKG5QGUTW04	AKG5QGUTW03
	Micron MT51J256M32HF-70:A	AKG5QGUTL07	AKG5QGUTL06
	Samsung K4G80325FB-HC28	AKG5QGD509	AKG5QGD508



N16S strap setting	
ROM_SI	VRAM Configuration follow VRAM table
ROM_SD	Stuff 4.98G Pull Up CS14892P826
ROM_SCLK	Stuff 4.98G Pull Down CS14892P826
STRAP0	Stuff 49.9K Pull Up CS14892P810
STRAP1	NC
STRAP2	NC
STRAP3	NC
STRAP4	NC
STRAP5	NC
N17S strap setting	
ROM_SI	Stuff 100K Pull Up CS41002B820
ROM_SD	Stuff 100K Pull Up CS41002B820
ROM_SCLK	Stuff 100K Pull Up and 100K Pull Down CS41002B820
STRAP0	VRAM Configuration follow VRAM table
STRAP1	VRAM Configuration follow VRAM table
STRAP2	VRAM Configuration follow VRAM table
STRAP3	Stuff 100K Pull Down CS41002B820
STRAP4	Stuff 100K Pull Down CS41002B820
STRAP5	Stuff 100K Pull Down CS41002B820

	STRAP2	STRAP1	STRAP0	
Samsung	L	L	L	0x0000
Micron	H	L	L	0x0004
Hynix	H	L	H	0x0005

STRAP[2:0] VRAM Table for N17S-G1 GDDR5 Recommended Memories

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N
0x0	GDDR5 512Mx16 7 GHz	Samsung B die	K4G80325FB-BC28	AKG5QGDT509	AKG5QGDT508
0x4	GDDR5 512Mx16 8 GHz	Micron B die	MT51J256M32HF-80:B	AKG5QGUTL24	AKG5QGUTL25
0x5	GDDR5 512Mx16 8 GHz	Hynix A die	H5GC8H24AJR-R2C	AKG5QGUTW15	AKG5QGUTW16

ROM_SI VRAM Table for N16S-GTR GDDR5 Recommended Memories

ROM_SI	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N
0x0	GDDR5 512Mx16 7 GHz	Samsung B die	K4G80325FB-BC28	AKG5QGDT509	AKG5QGDT508
0x8	GDDR5 512Mx16 8 GHz	Micron B die	MT51J256M32HF-80:B	AKG5QGUTL24	AKG5QGUTL25
0x9	GDDR5 512Mx16 8 GHz	Hynix A die	H5GC8H24AJR-R2C	AKG5QGUTW15	AKG5QGUTW16

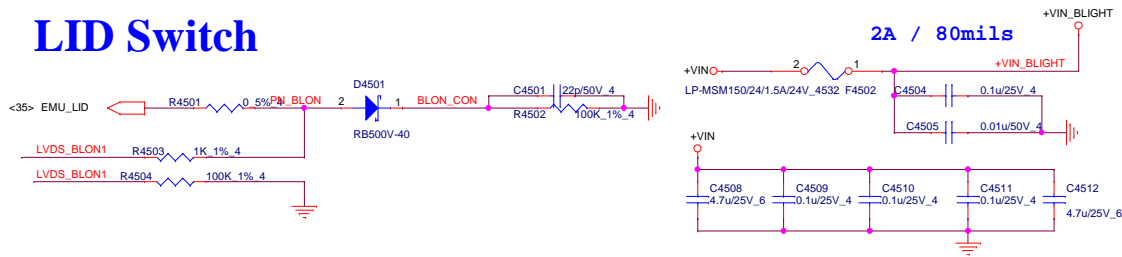
R1055	SAMSUNG	0000	4.98G	CS24992P826
R1046	HYUNIX	1001	4.98G	CS11002P826



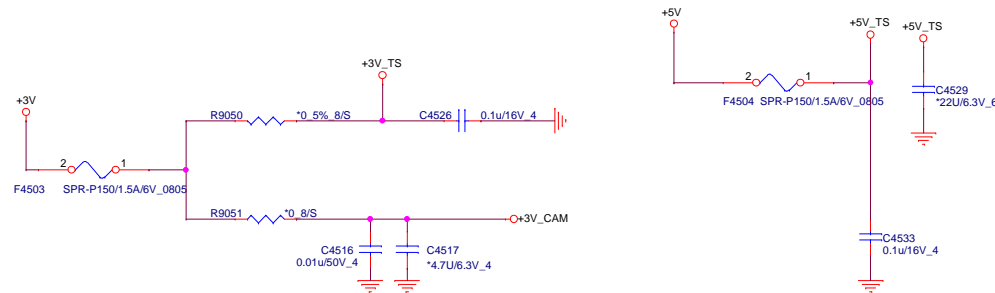
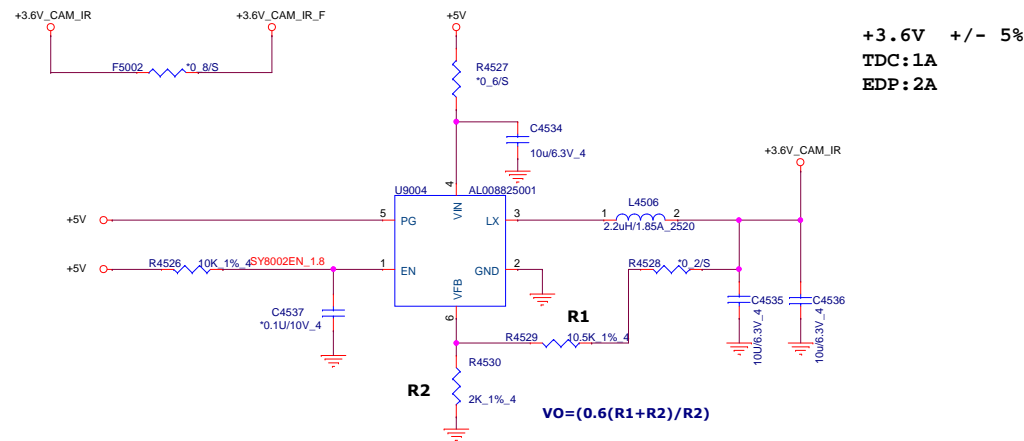
PROJECT : G7BD
Quanta Computer Inc.

Rev	Document Number	Rev
Ctrlm	24 -- VRAM CONFIG	1A
Date:	Wednesday, December 26, 2018	Sheet 24 of 49

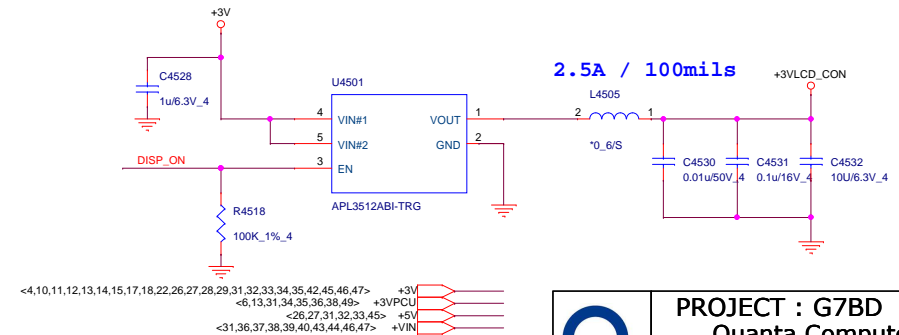
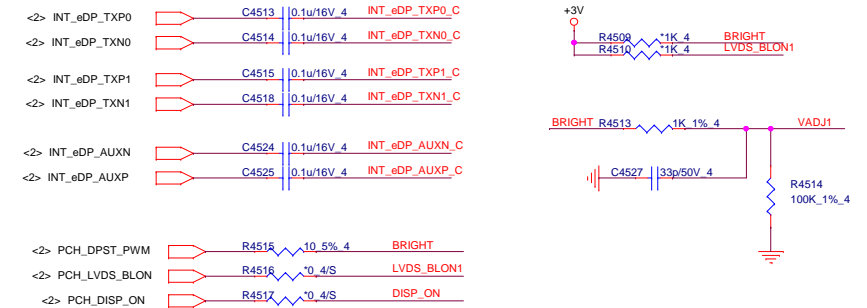
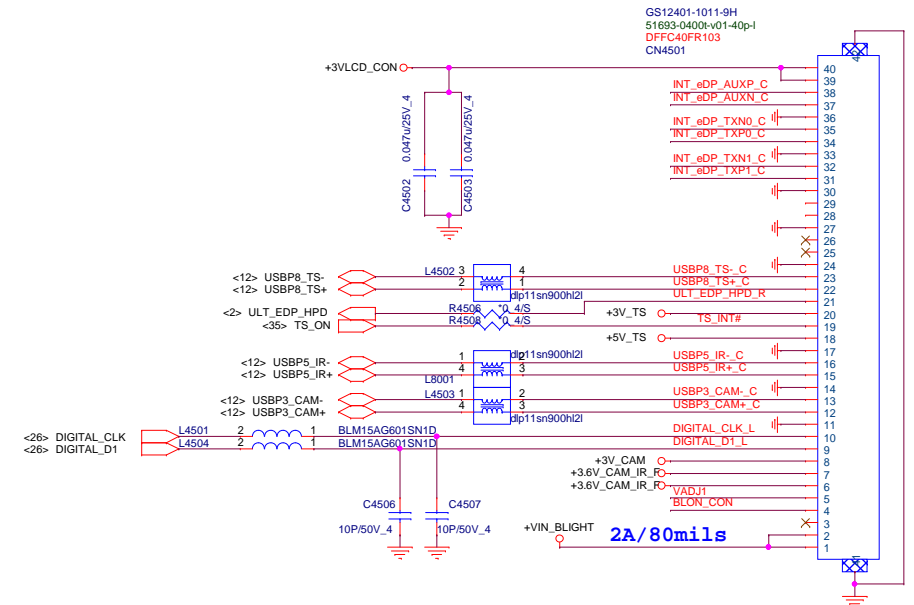
LID Switch

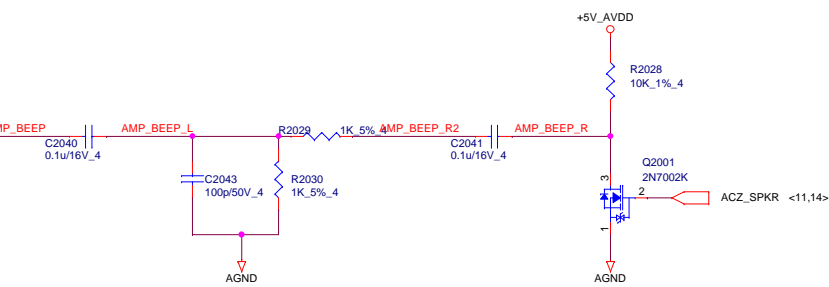
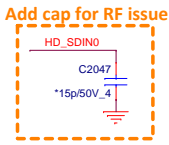
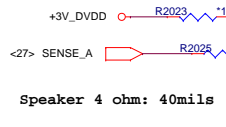
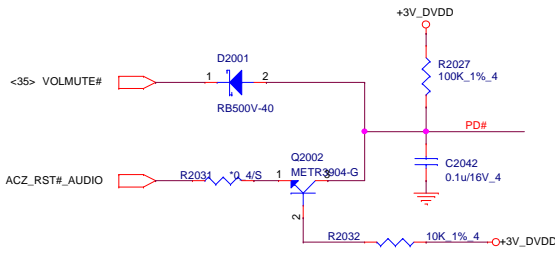
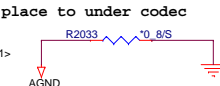
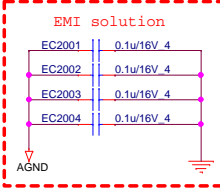
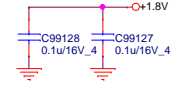
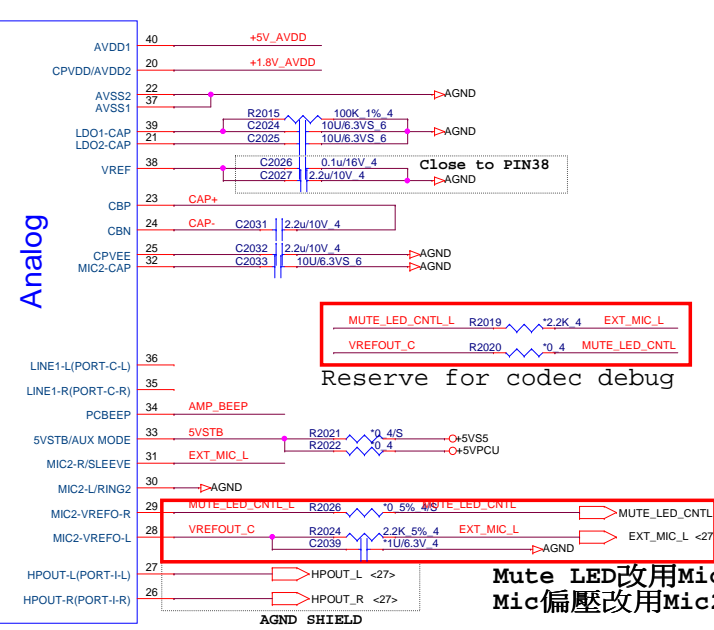
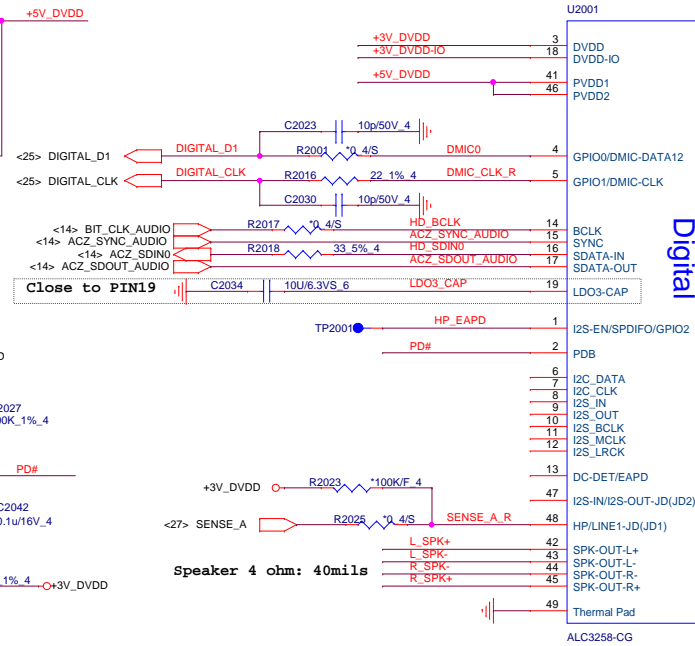
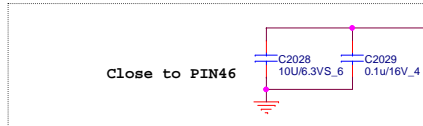
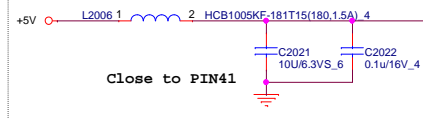
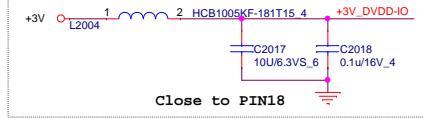
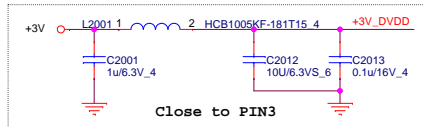


Touch screen

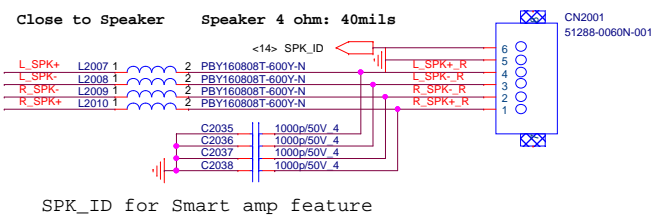
**IR CAM**

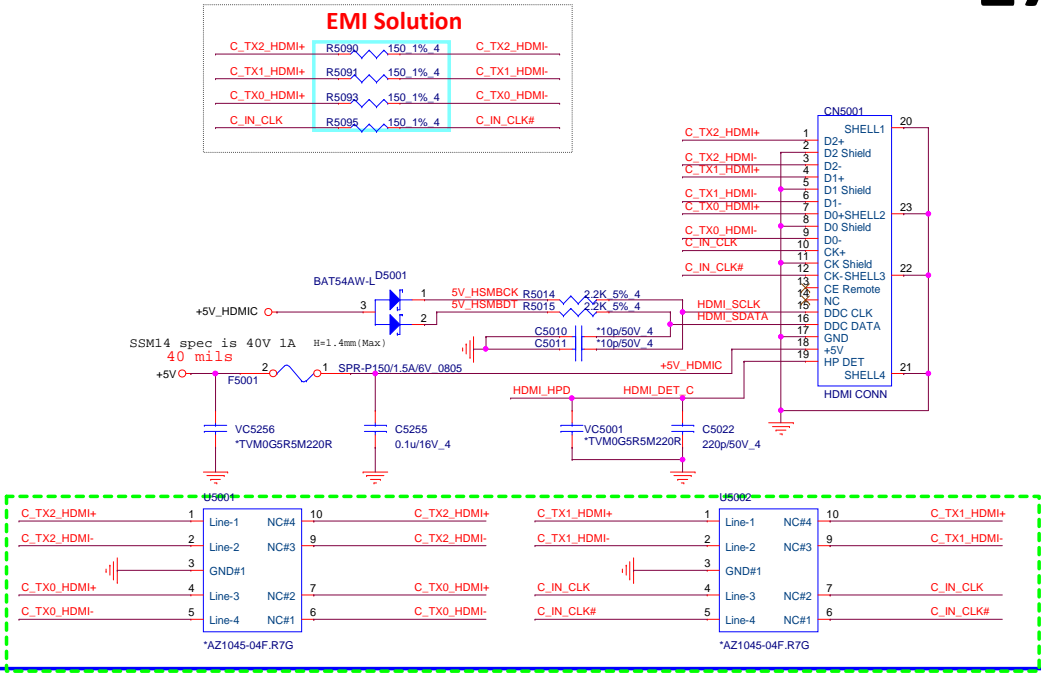
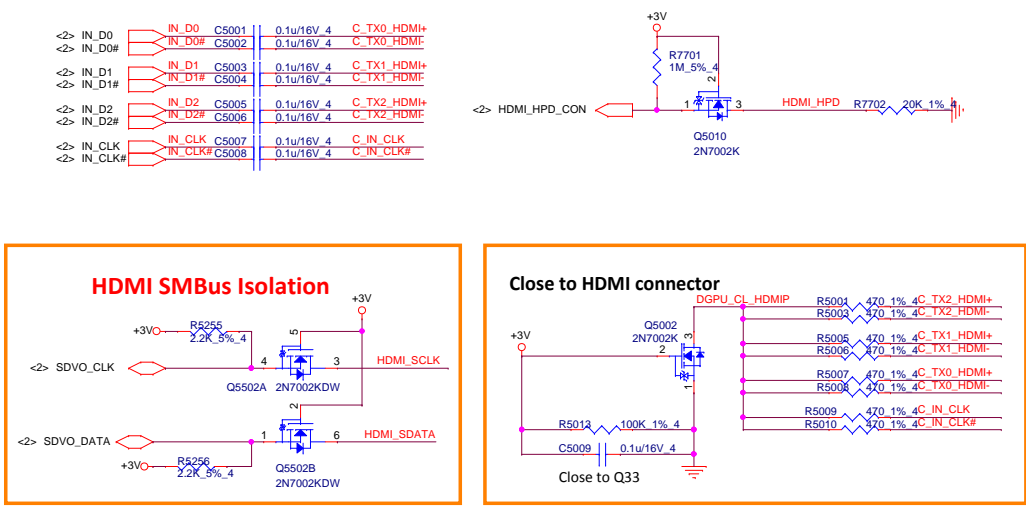
eDP Conn.



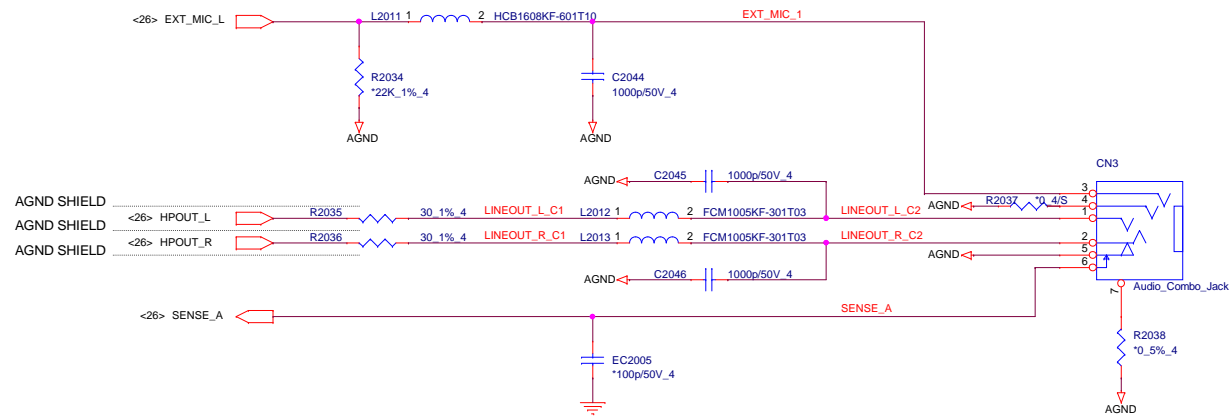


SPK CONN

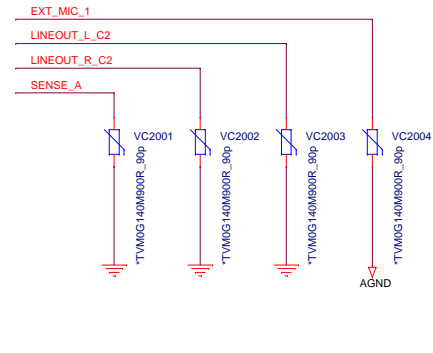




Audio Jack



Audio JACK ESD



LAN RTL8111HSH-CG

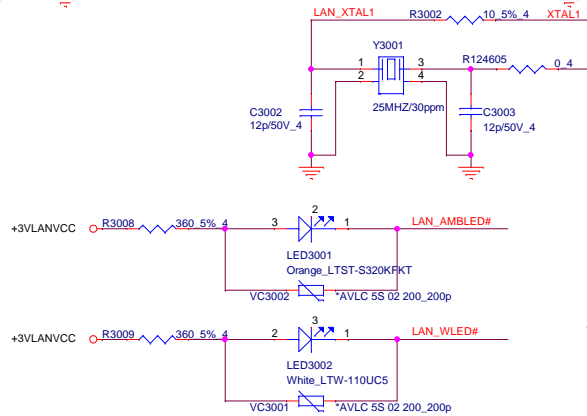
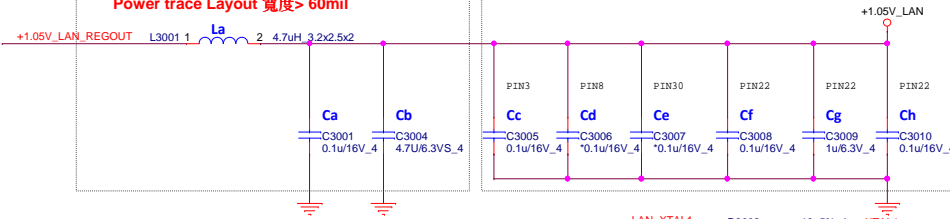
28

For SWR mode support
RTL8107ESH-CG/RTL8111HSH-CG
Stuff: La, Ca, Cb

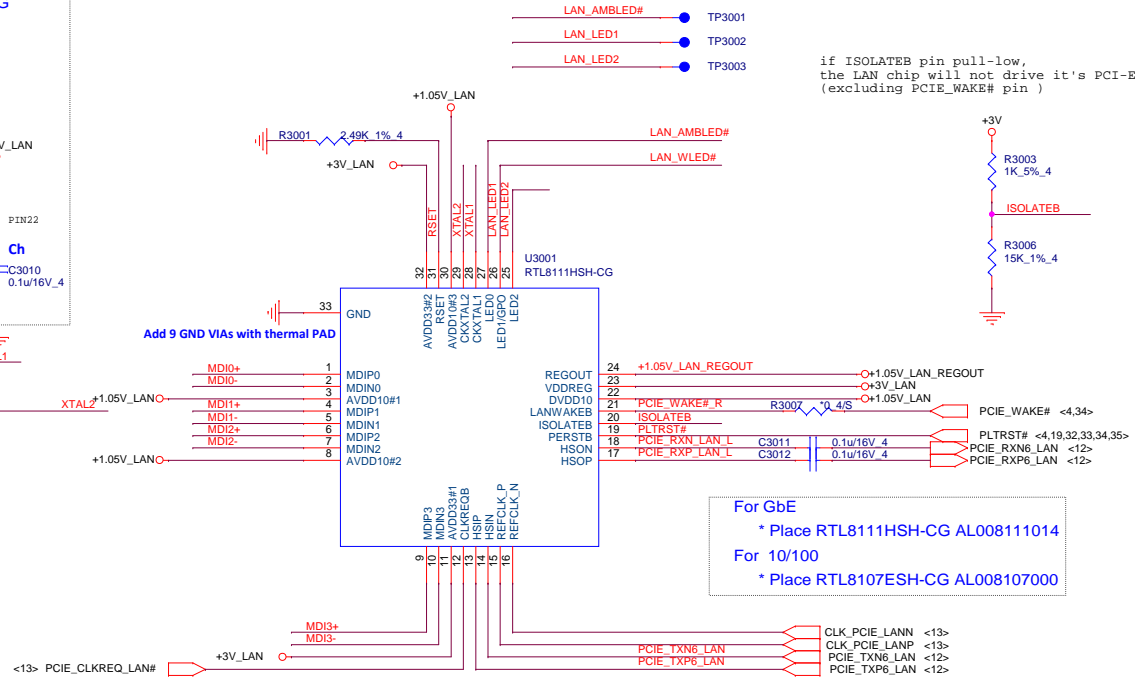
* Place Cc,Cd,Ce,Cf for RTL8107ESH-CG/RTL8111HSH-CG
close to each VDD10 pin-- 3, 22, 8, 30

* Place Cg,Ch for RTL8107ESH-CG/RTL8111HSH-CG
close to each VDD10 pin-- 22(reserved)

Power trace Layout 宽度> 60mil



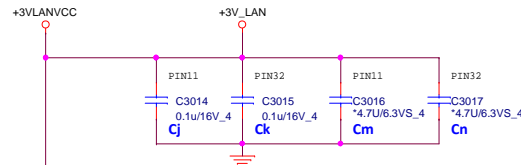
Add 9 GND VIAs with thermal PAD



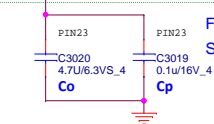
For GbE
* Place RTL8111HSH-CG AL008111014
For 10/100
* Place RTL8107ESH-CG AL008107000

* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for
RTL8107ESH-CG/RTL8111HSH-CG

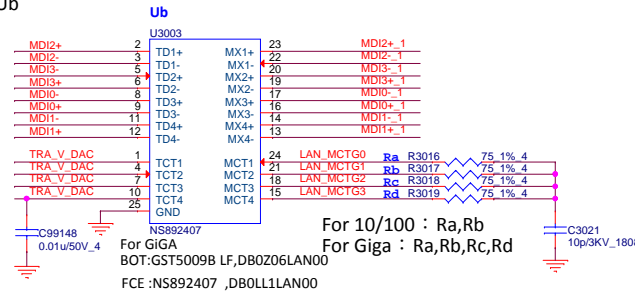
* For surge improvement, place Cm and Cn, close to each
VDD33 pin-- 11, 32(optional)



For SWR mode support RTL8107ESH-CG/RTL8111HSH-CG
Stuff Co, Cp

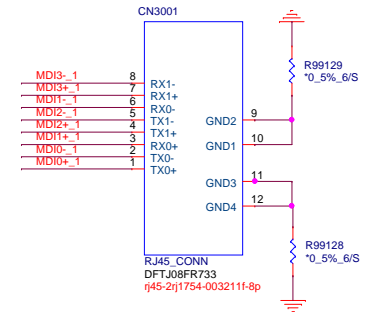


For Giga : Ub



For 10/100 : Ra,Rb
For Giga : Ra,Rb,Rc,Rd

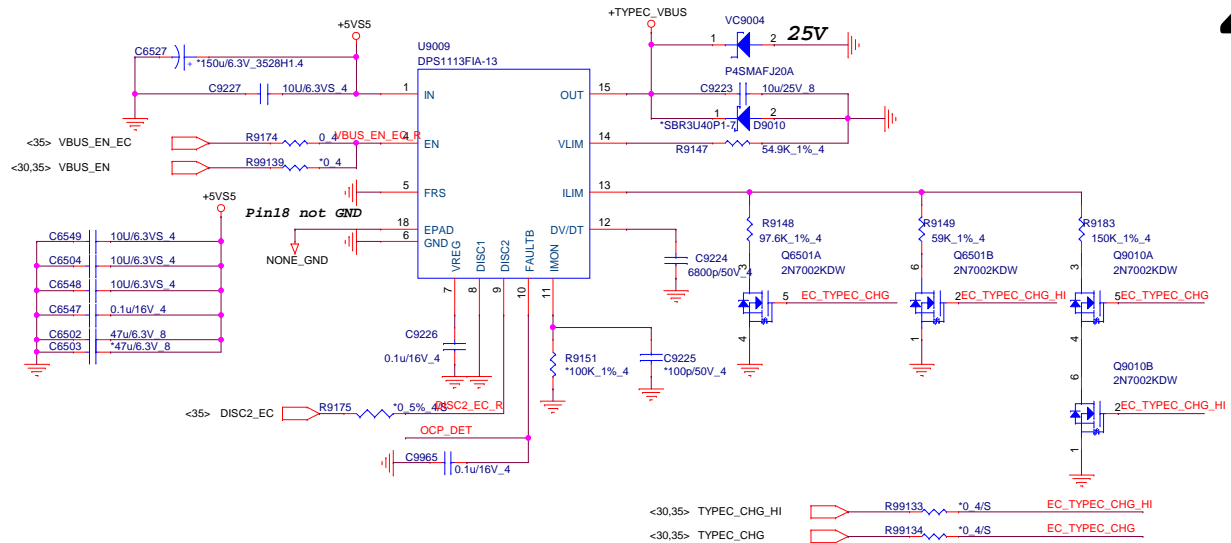
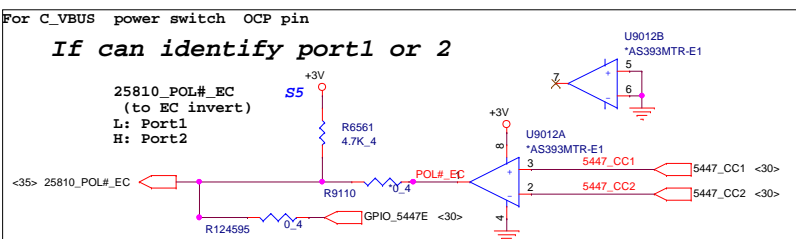
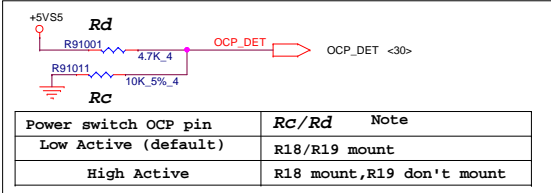
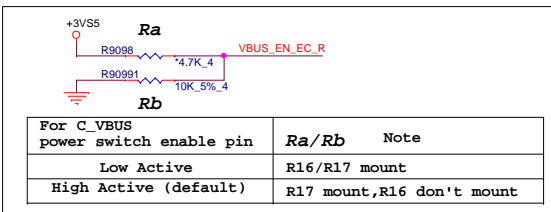
RJ45



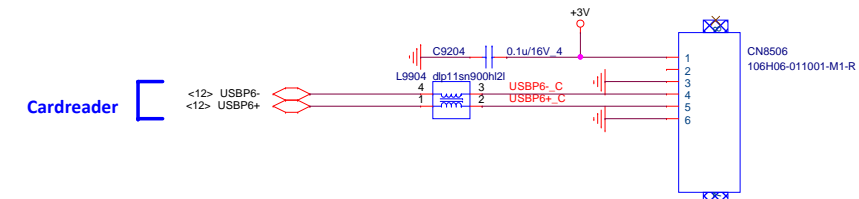
PROJECT : G7BD		
Quanta Computer Inc.		
Size Custom	Document Number 30 -- LAN RTL8166EH/RTL8111HSH	Rev 1A
Date: Wednesday, December 26, 2018 Sheet 28 of 49		

USB TYPEC POWER SWITCH

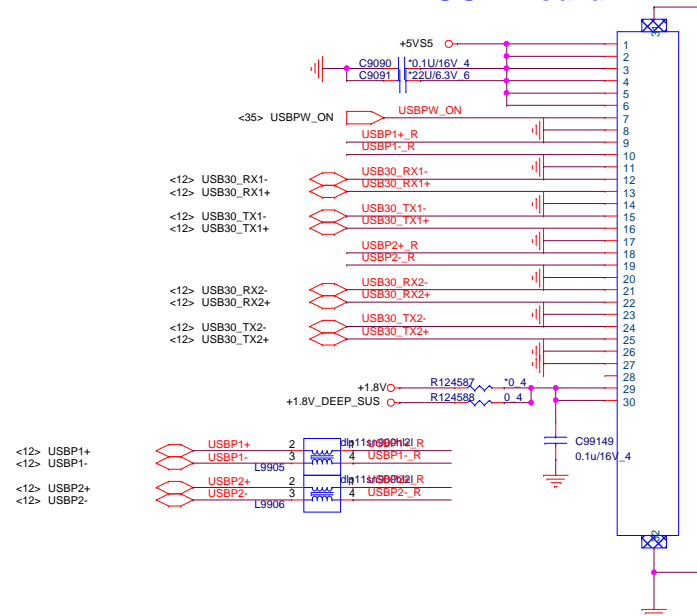
29



SD Board



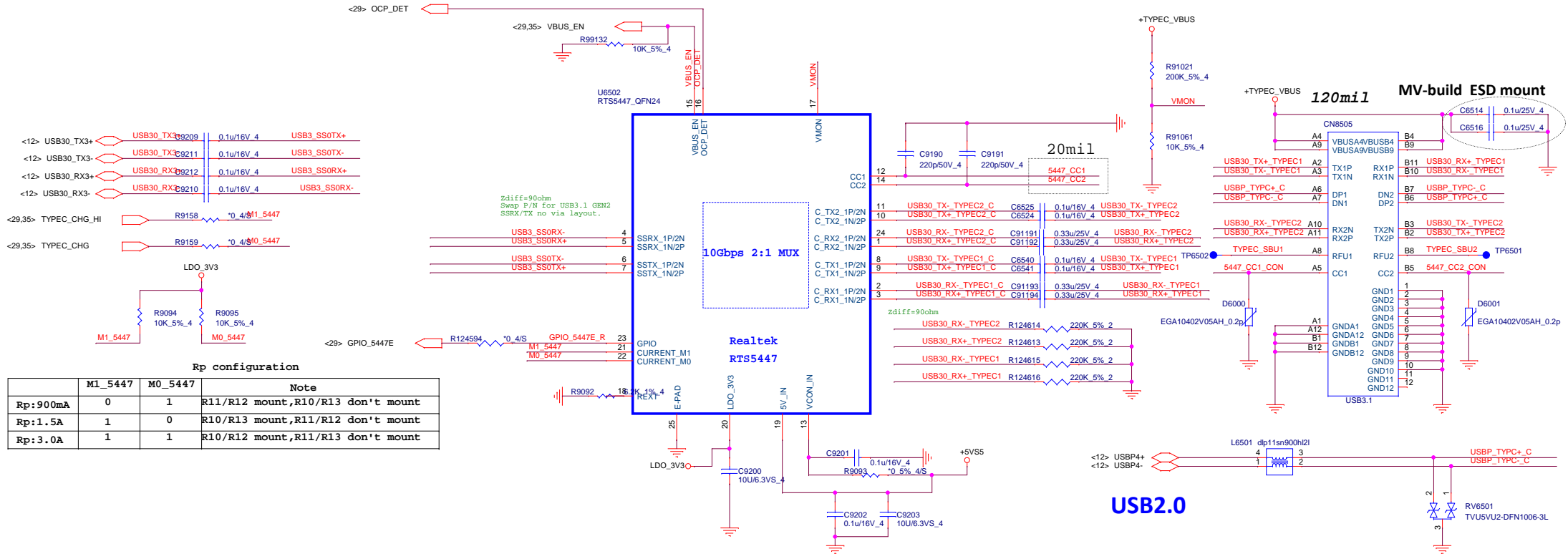
USB Board



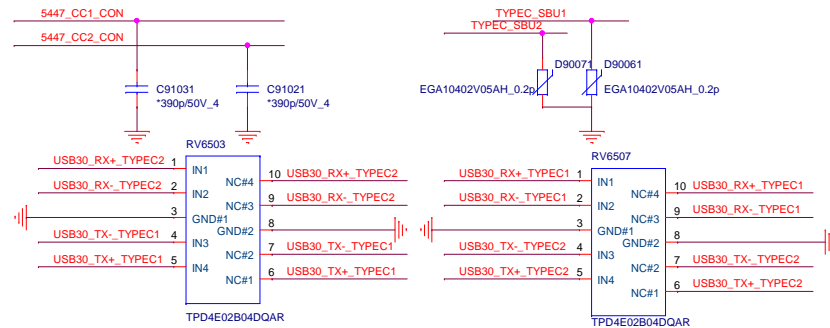
TYPE C MUX RTS5447

<4,26,29,32,33,37,38,39,40,41,42,43,45,46,47,48> +5VS5
<4,12,13,15,29,32,33,34,35,38,39,40,41,45,48> +3VS5
<4,10,11,12,13,14,15,17,18,22,25,26,27,28,29,31,32,33,34,35,42,45,46,47> +3V
<29> +TYPEC_VBUS

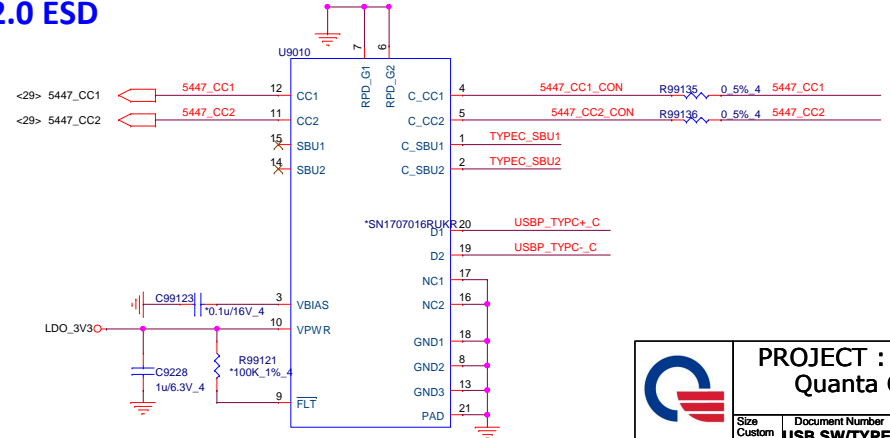
30



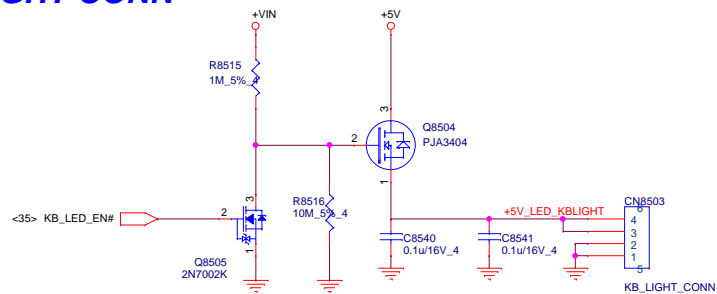
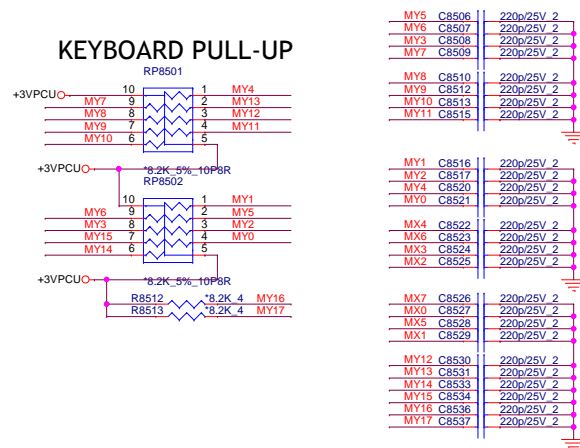
TYPE C USB3.0 ESD



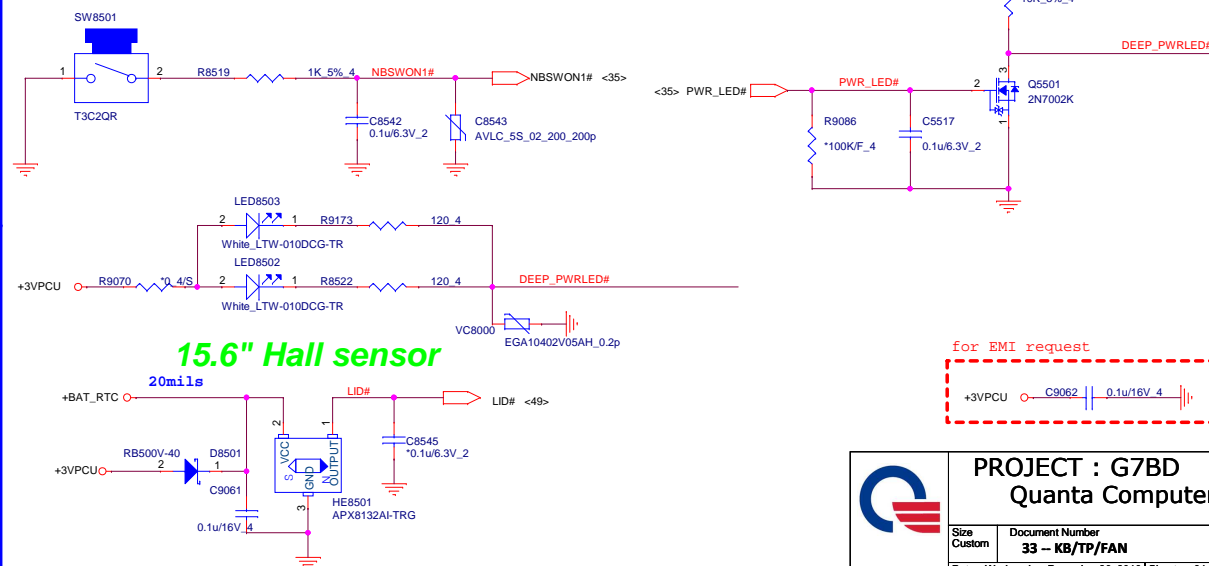
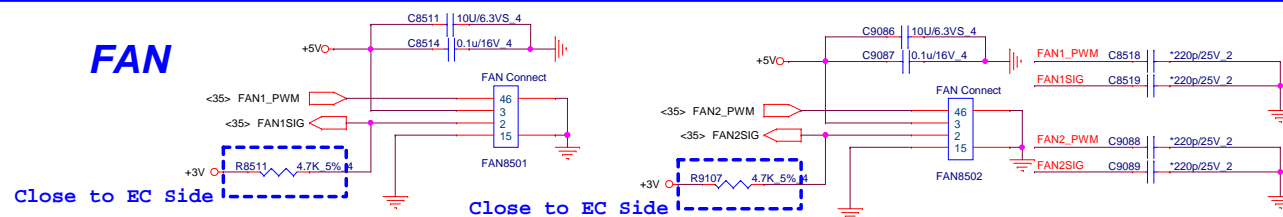
TYPE C USB2.0 ESD



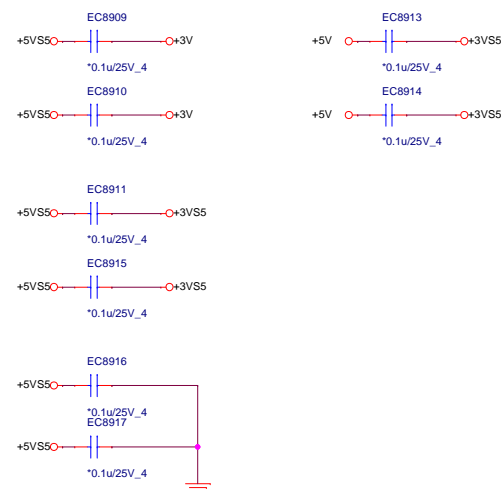
KB LIGHT CONN



PWR Button & LED & HALL IC

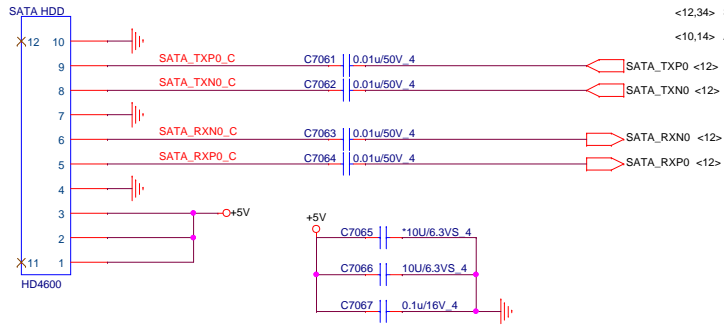


change to FW 5.6 I
PN:AL009665013



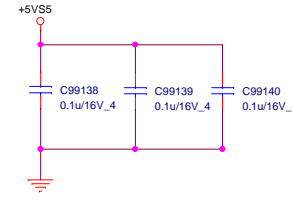
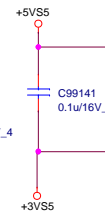
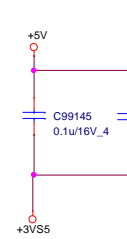
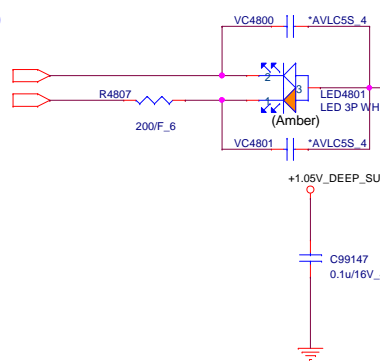
SATA HDD & LED

SATA LED

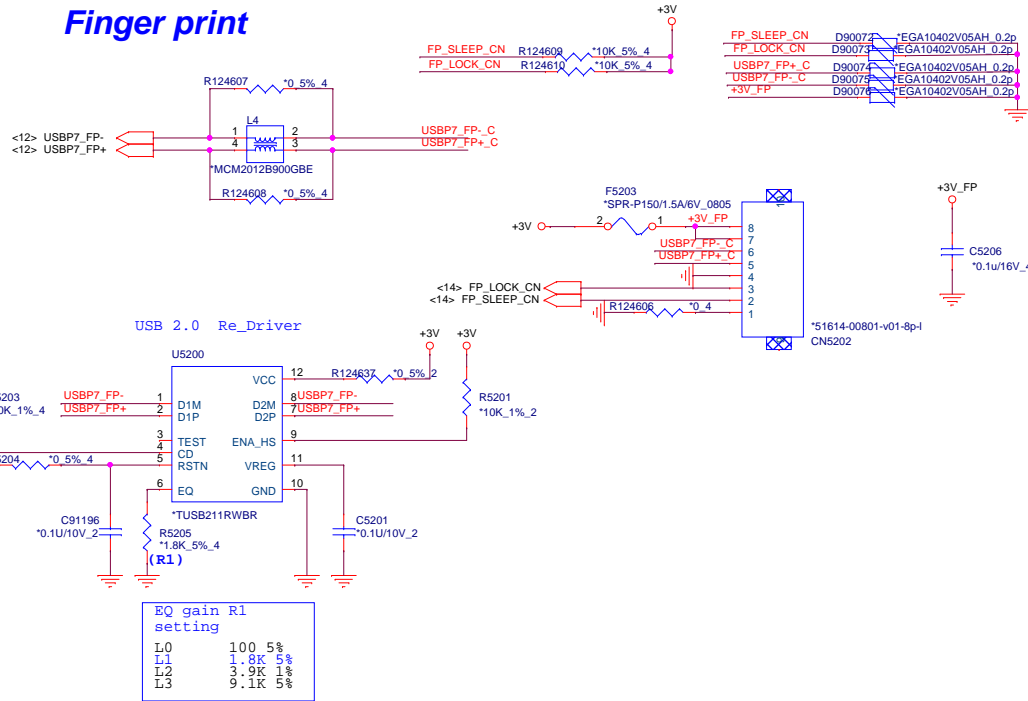


<12,34> SATA_LED#

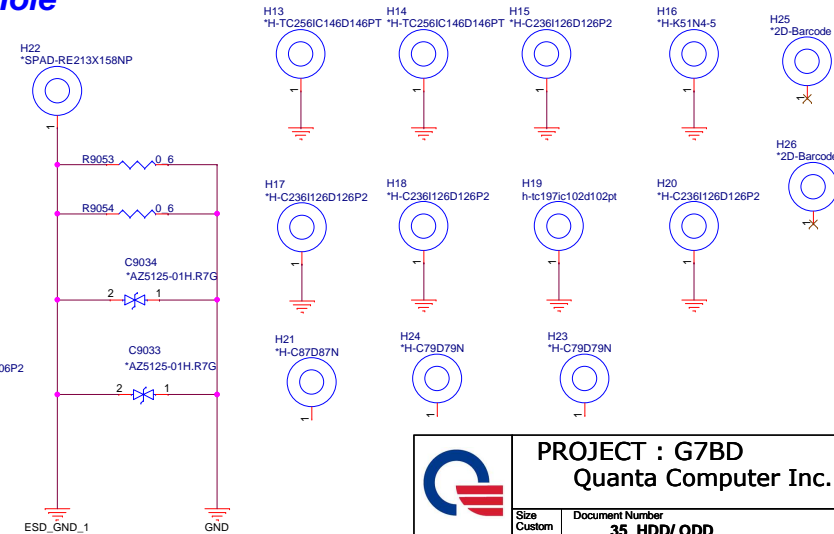
<10,14> ACC_LED#



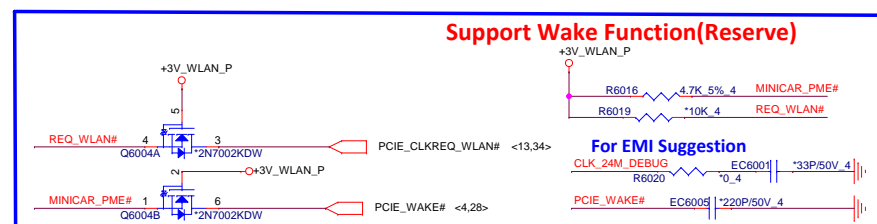
Finger print

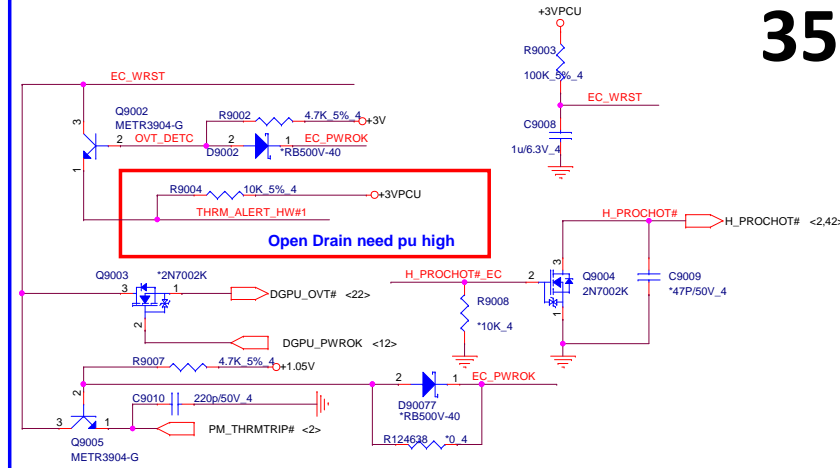
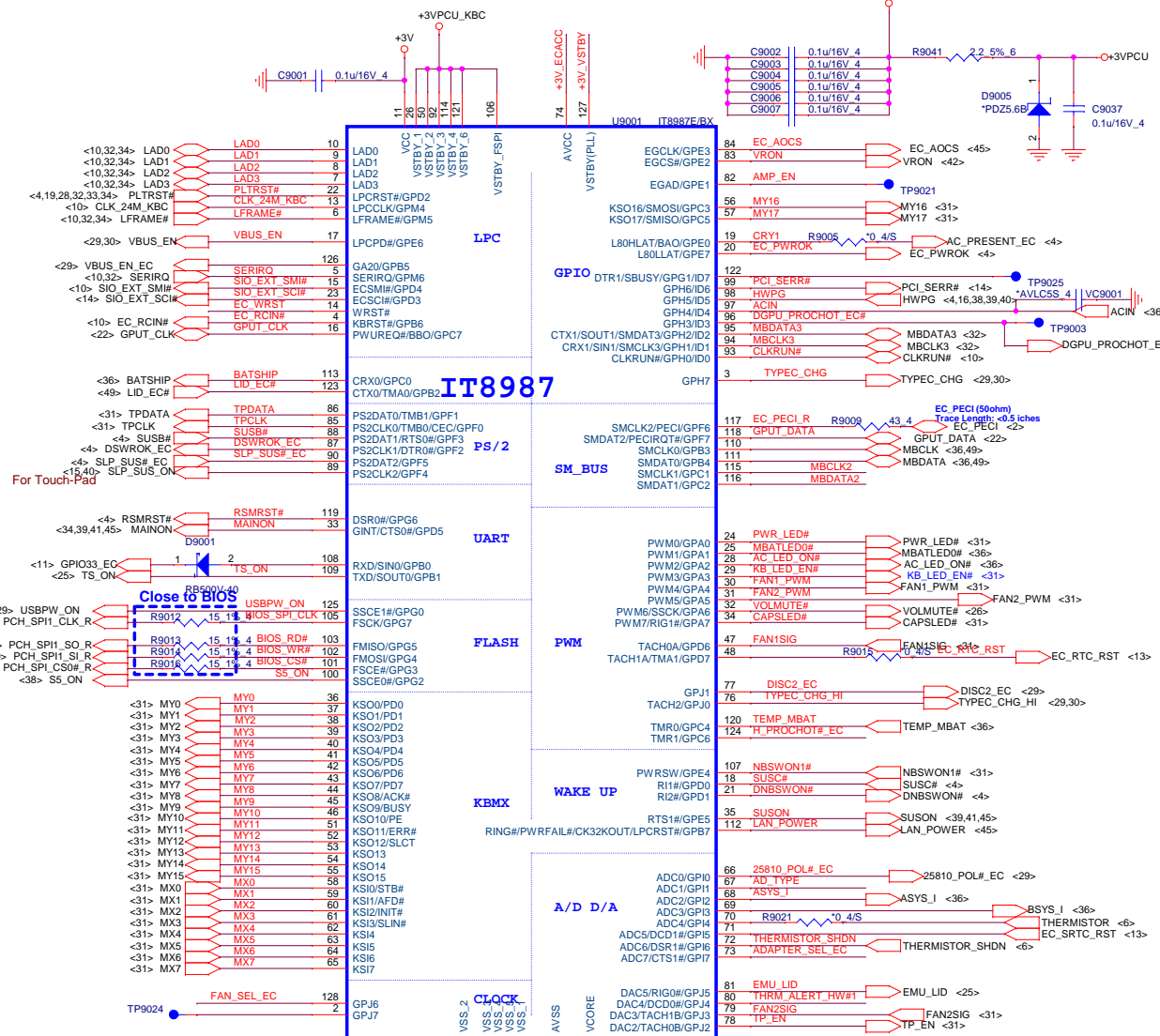


Hole



34

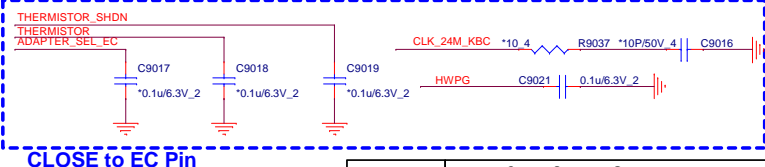
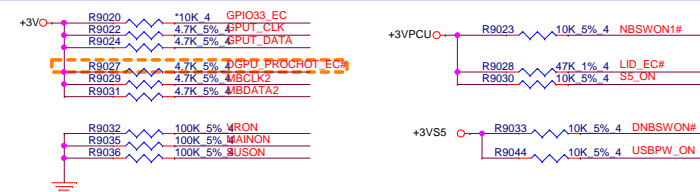
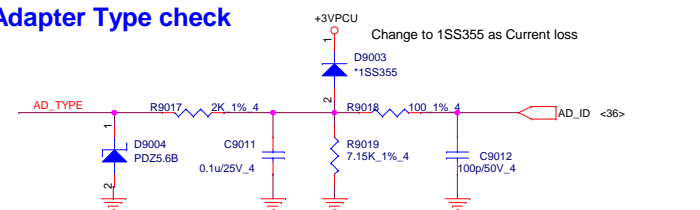
[illegible]



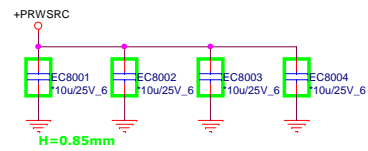
Adapter select for EC

	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002FB26)	100K (CS41002FB28)	3V	
150W	10K(CS31002FB26)	100K (CS41002FB28)	3V	
120W	10K(CS31002FB26)	21.5K(CS32152FB09)	2.25V	
90W	10K(CS31002FB26)	8.25K(CS28252FB07)	1.5V	
65W	10K(CS31002FB26)	2.94K(CS22942FB01)	0.75V	DIS
45W	NC	10K(CS31002JB28)	0V	UMA

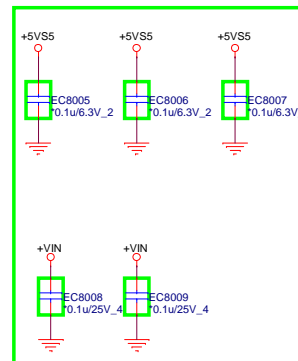
Adapter Type check




Acoustic Solution



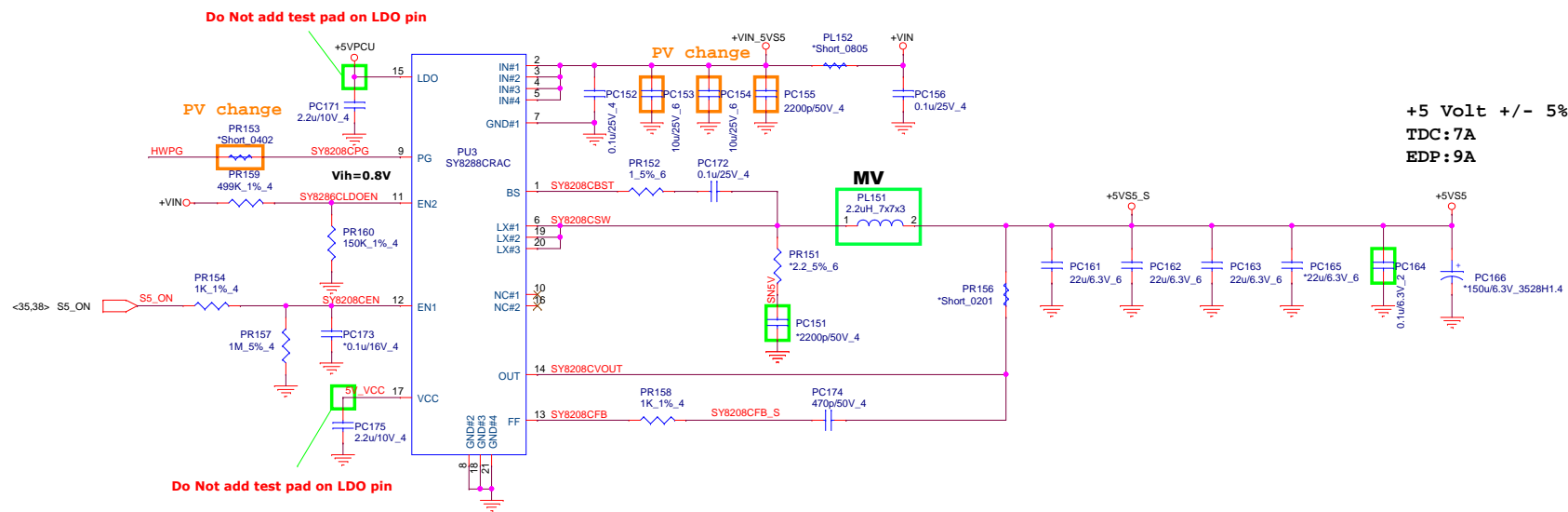
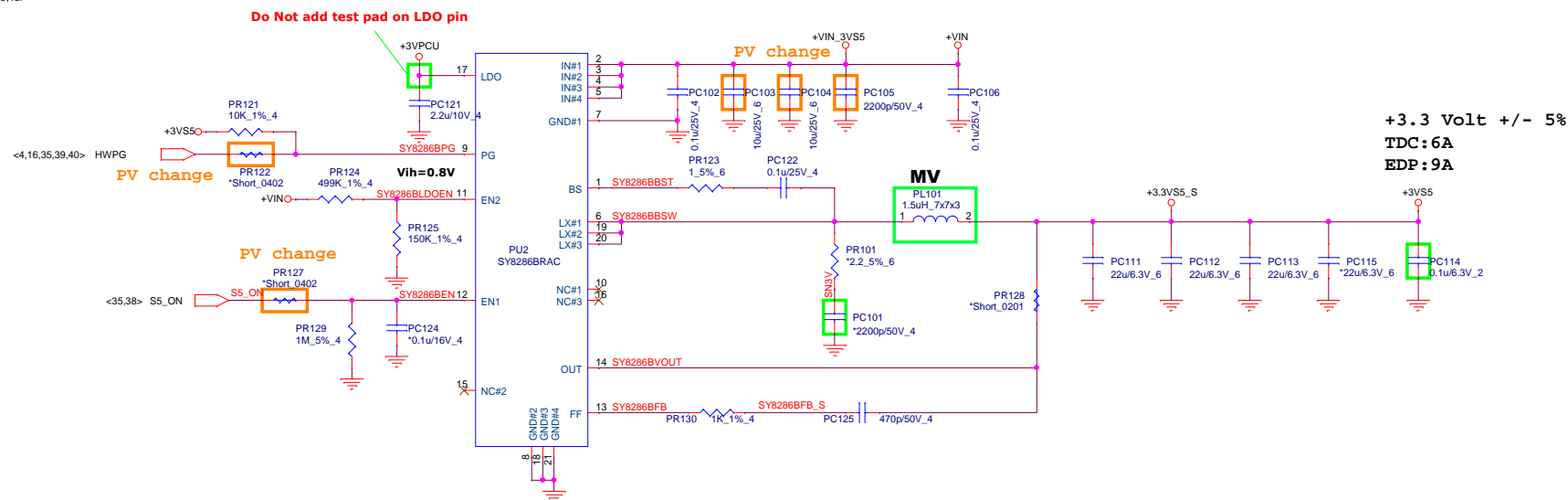
EMI suggestion to reserve

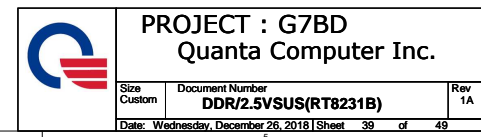


DC/DC +3VS5/+5VS5



+VIN <25,31,36,37,39,40,43,44,46,47>
 +3VS5 <4,12,13,15,29,32,33,34,35,39,40,41,45,48>
 +5VS5 <4,26,29,30,32,33,37,39,40,41,42,43,45,46,47,48>
 +3VPCU <6,13,31,34,35,36,49>
 +5VPCU <26,34,36,45,48>



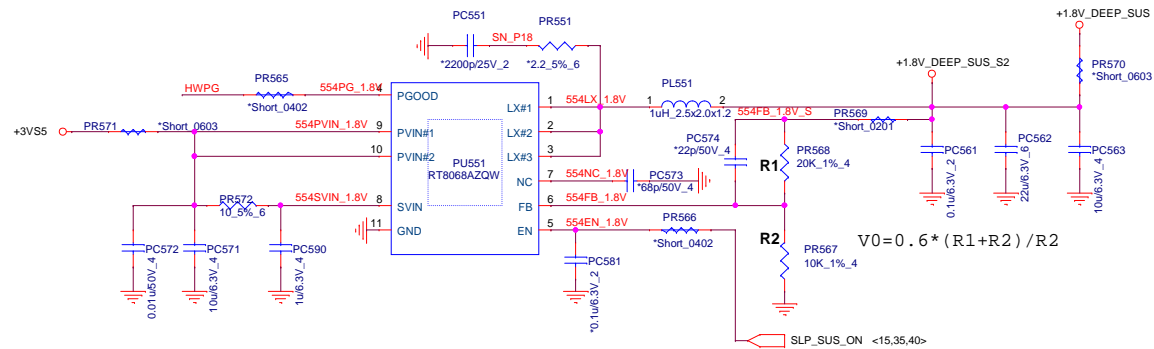


(V1.00A+V1.00_MODPHY+VccPRIM_CORE)
+1.0V5S Volt +/- 5%
Countinue current:6A
Peak current:9A

MV
PL501
2.2uH_7x7x3

Vout1=(1+R1/R2)*0.8

1.8VS5 +/- 3%
TDC:3A
EDP:4A



Volume Segment

SKY/KBY-U22/U42/U23e
KBY-G/WHL-U
Vcc_IO: 3.4A/1V
Stuff PU601

Volume Segment

SKY/KBY-H 22/42/44e

Vcc_IO: 5.5A/0.95V

Stuff PU601 & merge 1V_deep_sus

Volume Segment

CNL U22

Vcc_IO: 5.1A/0.95V

Vcc_IO: Can merge +1.05V_deep_sus

Unstuff PU603

Default setting

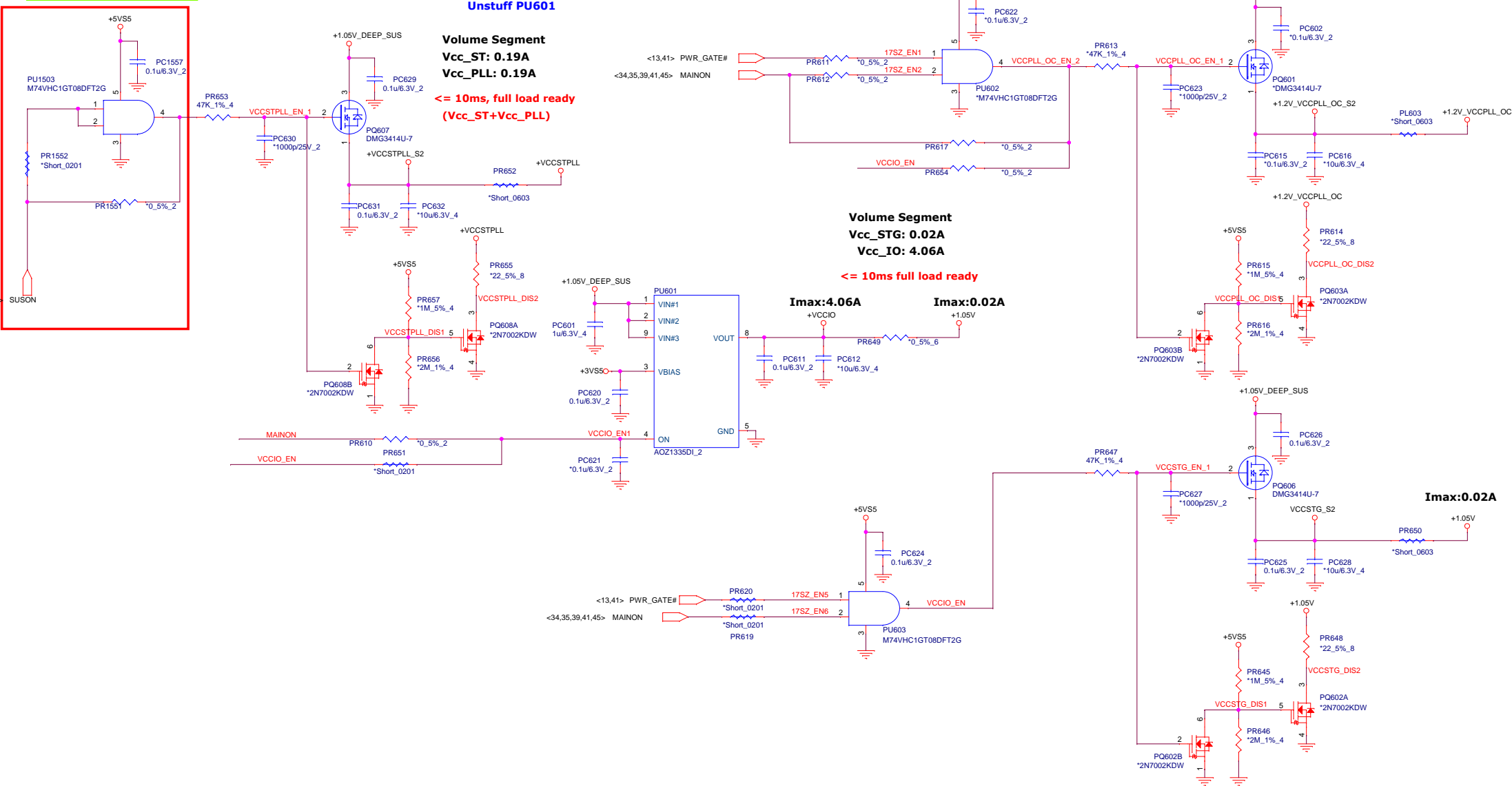
Volume Segment

CFL H6/H4

Vcc_IO: 6.4A/0.95V

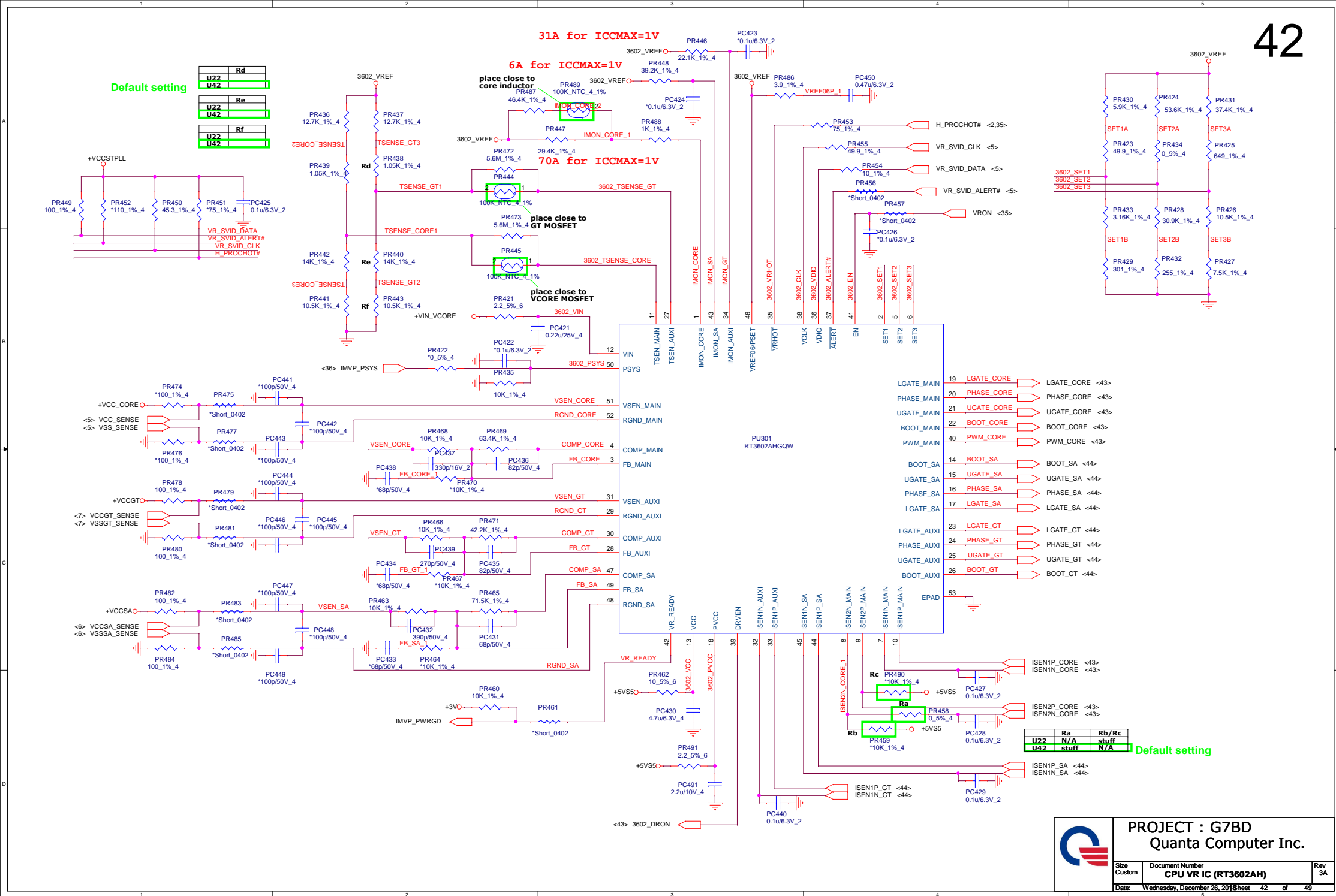
Stuff PU603

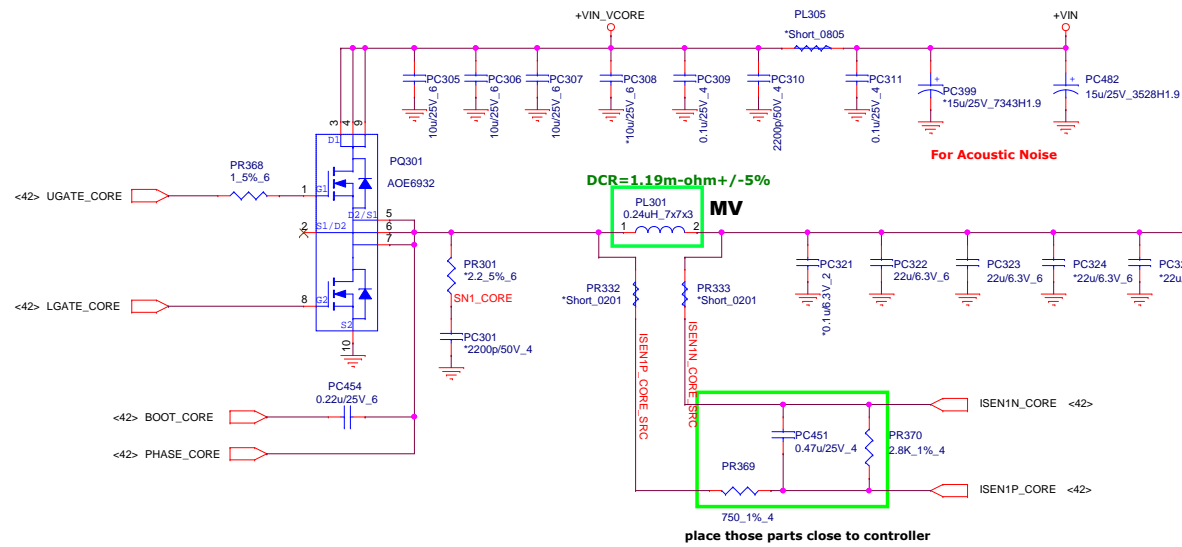
Unstuff PU601



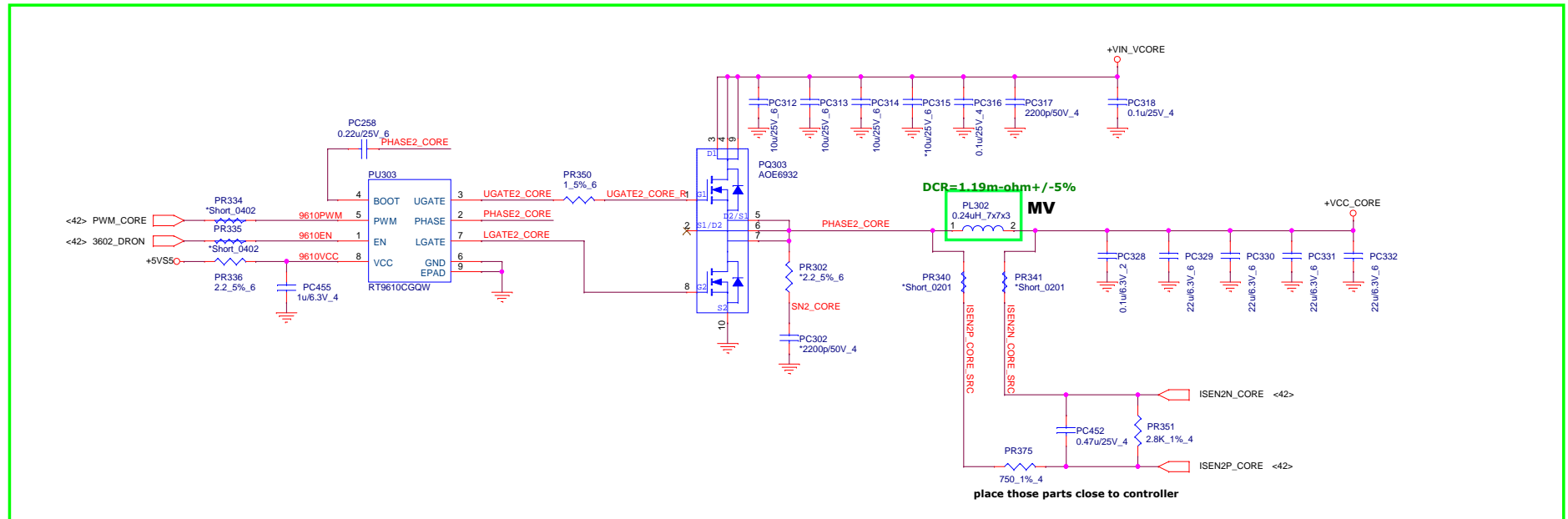
PROJECT : G7BD
Quanta Computer Inc.

Size Custom	Document Number +1.0V/+VCCSTPLL	Rev 1.
Date: Wednesday, December 26, 2018 Sheet 41 of 49		

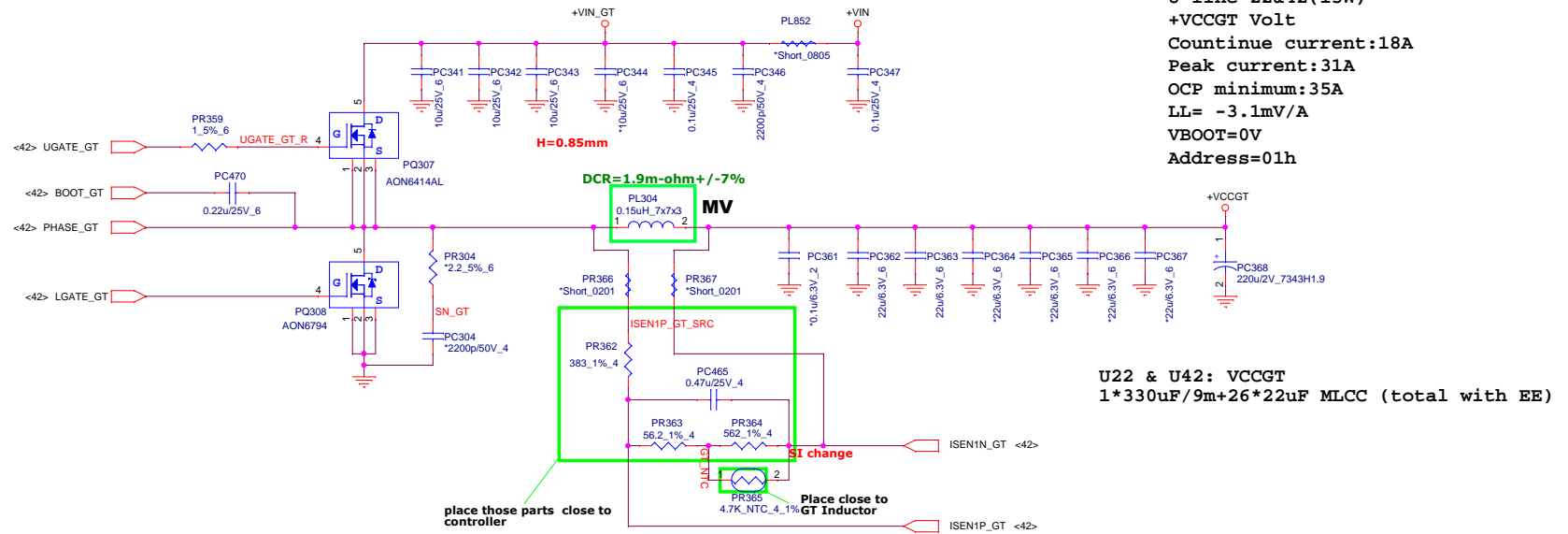
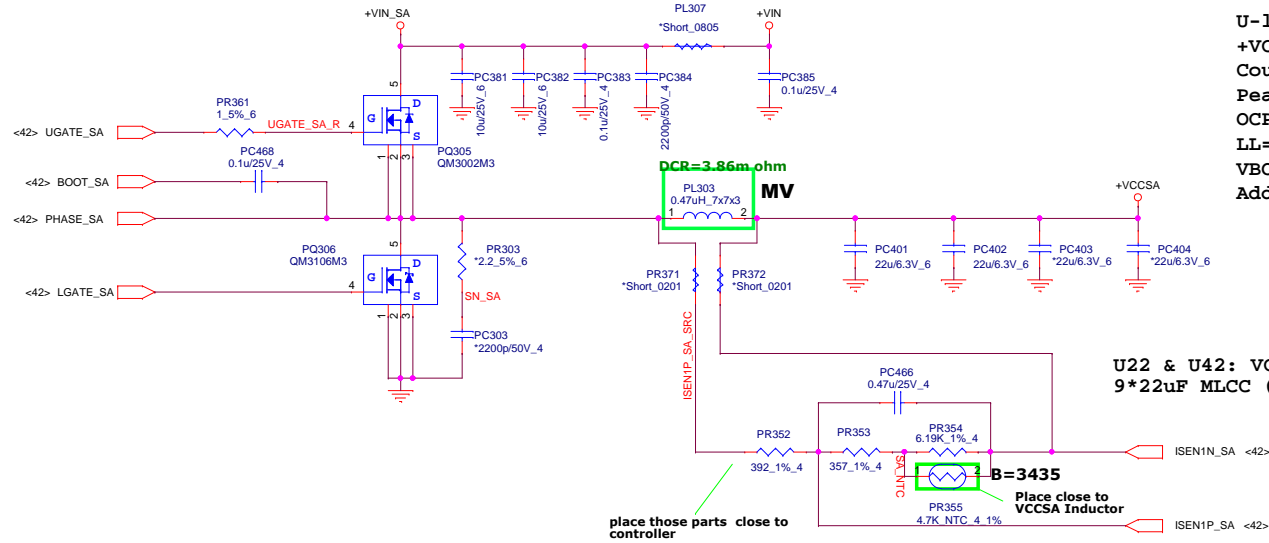


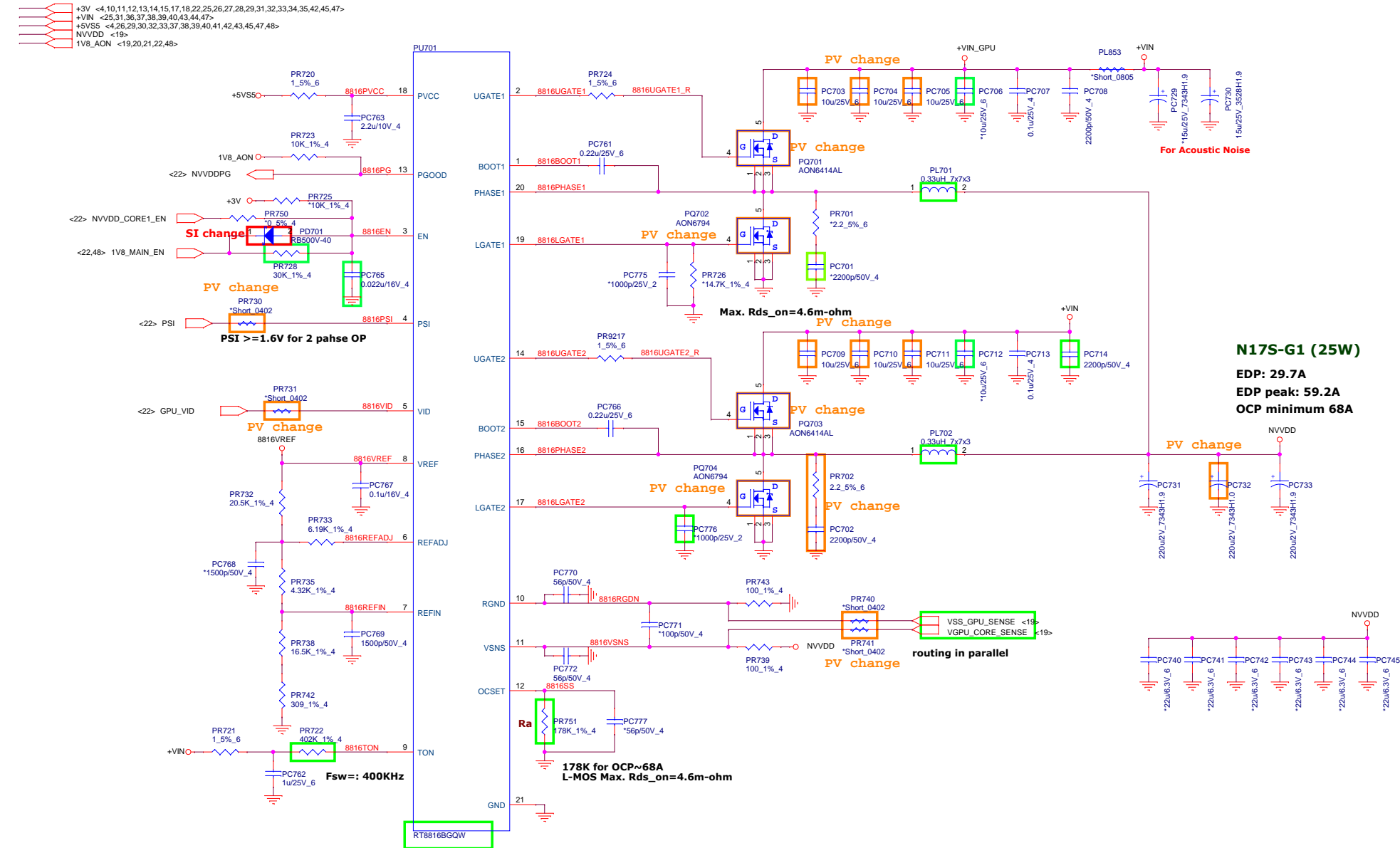


WHL U42: +VCC_CORE
2*330uF/9m+33*22uF MLCC (total with EE)

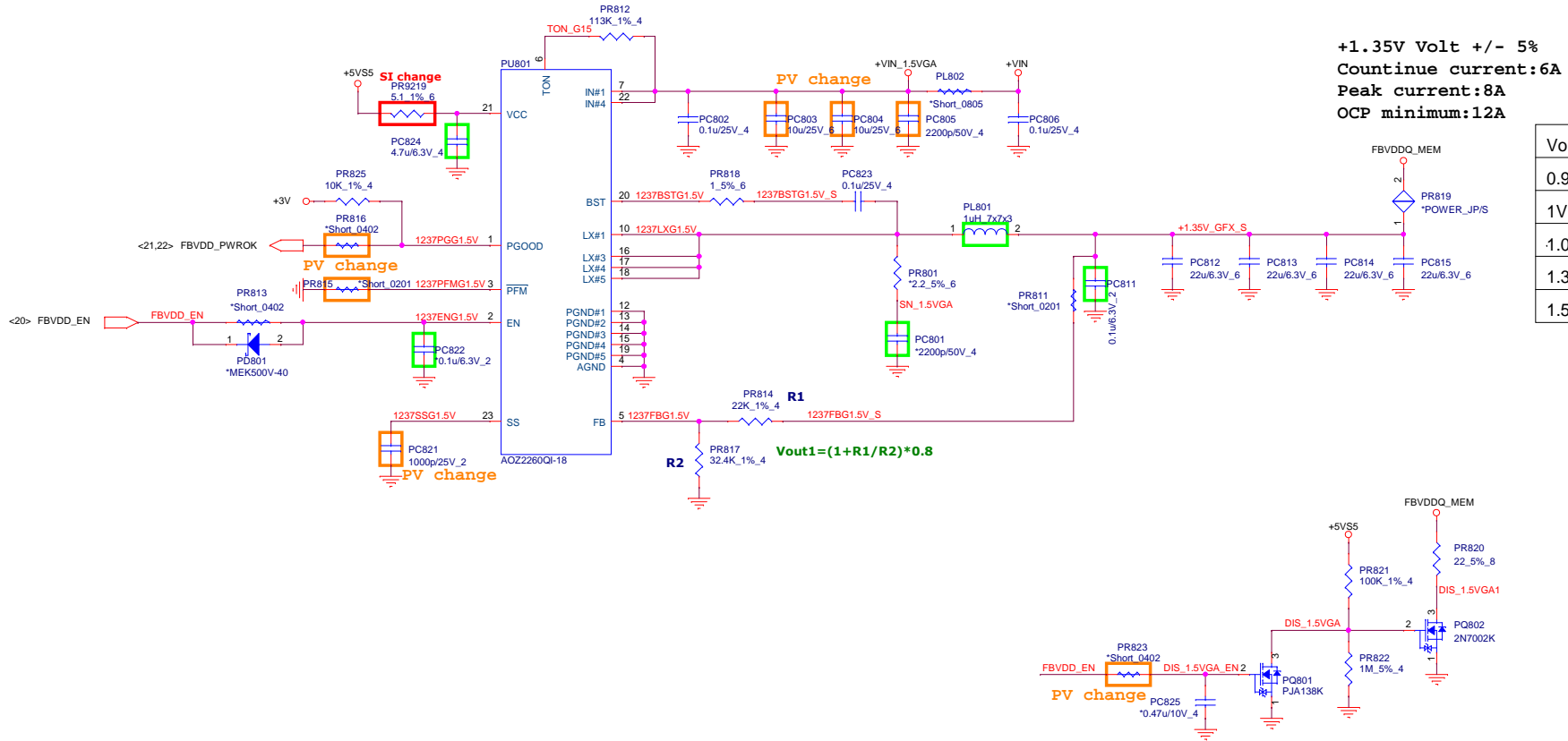


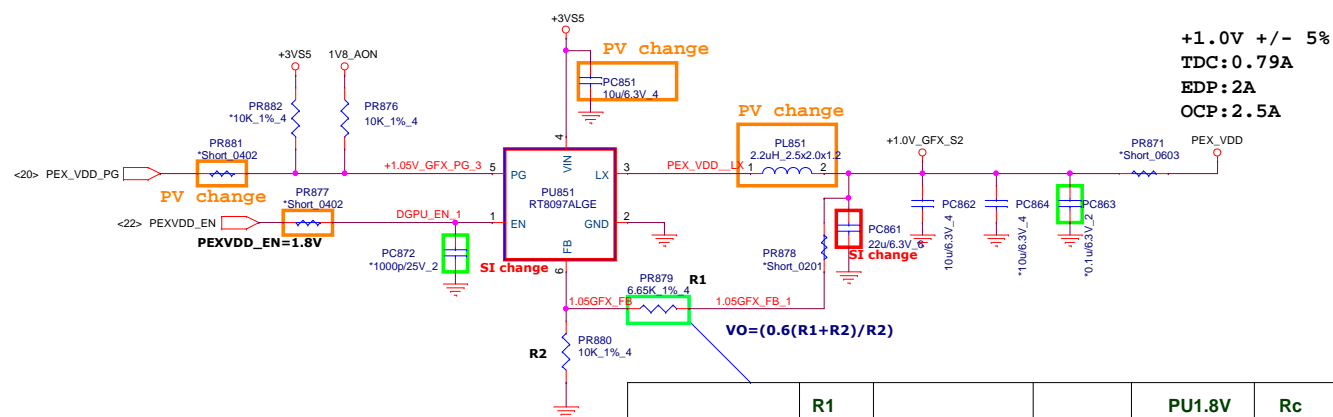
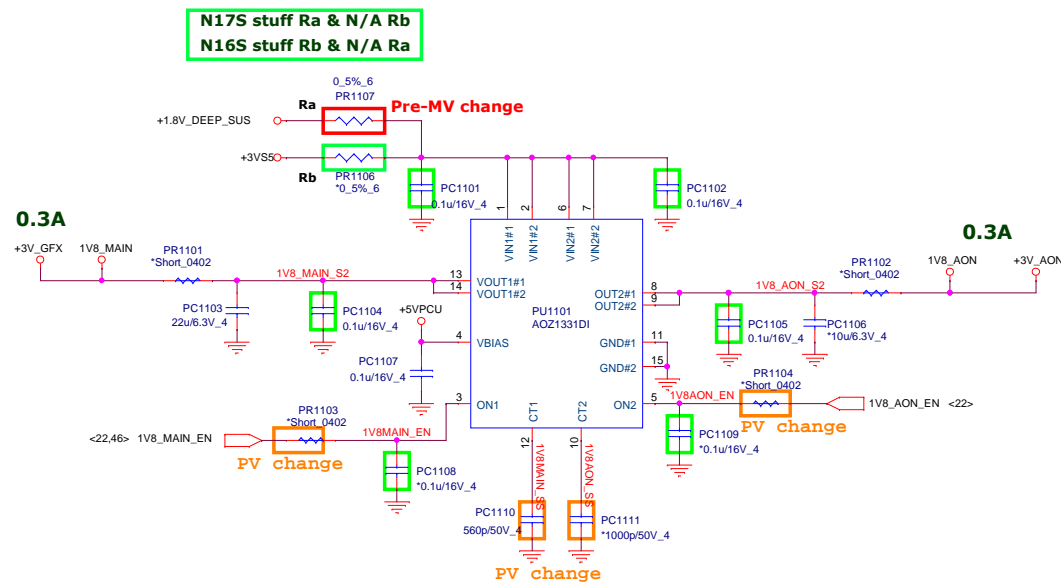
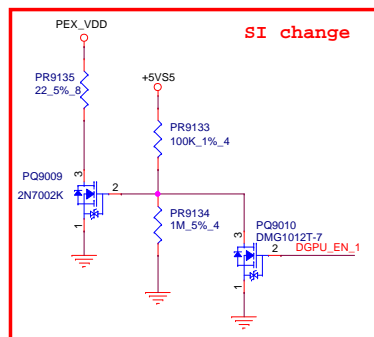
+VIN <25,31,36,37,38,39,40,43,46,47>
 +5VSS <4,26,29,30,32,33,37,38,39,40,41,42,43,45,46,47,48>
 +VCCSA <6,42>
 +VCCGT <7,42>





+VIN <25,31,36,37,38,39,40,43,44,46>
 +5VS5 <4,26,29,30,32,33,37,38,39,40,41,42,43,45,46,48>
 FBVDDQ_MEM <20,21,23>





	R1			PU1.8V	Rc	Rd
N17P N17S	6.65K	CS26652FB06	1V	Unstuff	Unstuff	Stuff
N16S GTR	7.5K	CS27502FB11	1.05V	Unstuff	Stuff	Unstu

